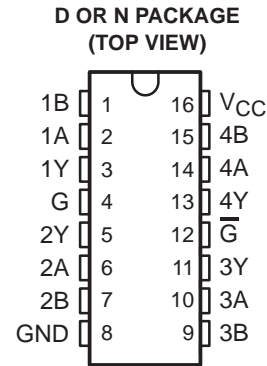


SN75ALS197 QUADRUPLE DIFFERENTIAL LINE RECEIVER

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- Meets or Exceeds the Requirements of ITU Recommendations V.10, V.11, X.26, and X.27
- Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments
- Designed to Operate Up to 20 Mbaud
- 3-State Outputs
- Common-Mode Input Voltage Range – 7 V to 7 V
- Input Sensitivity . . . ± 300 mV
- Input Hysteresis . . . 120 mV Typ
- High-Input Impedance . . . 12 k Ω Min
- Operates from Single 5-V Supply
- Low Supply-Current Requirement 35 mA Max
- Improved Speed and Power Consumption Compared to AM26LS32A



description

The SN75ALS197 is a monolithic, quadruple line receiver with 3-state outputs designed using advanced, low-power, Schottky technology. This technology provides combined improvements in bar design, tooling production, and wafer fabrication. This, in turn, provides significantly lower power requirements and permits much higher data throughput than other designs. The device meets the specifications of ITU Recommendations V.10, V.11, X.26, and X.27. It features 3-state outputs that permit direct connection to a bus-organized system with a fail-safe design that ensures the outputs will always be high if the inputs are open.

The device is optimized for balanced, multipoint bus transmission at rates up to 20 megabits per second. The input features high-input impedance, input hysteresis for increased noise immunity, and an input sensitivity of ± 300 mV over a common-mode input voltage range of –7 V to 7 V. It also features active-high and active-low enable functions that are common to the four channels. The SN75ALS197 is designed for optimum performance when used with the SN75ALS192 quadruple differential line driver.

The SN75ALS197 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each receiver)

DIFFERENTIAL INPUTS A–B	ENABLES		OUTPUT Y
	G	\bar{G}	
$V_{ID} \geq 0.3$ V	H	X	H
	X	L	H
-0.3 V < V_{ID} < 0.3 V	H	X	?
	X	L	?
$V_{ID} \leq -0.3$ V	H	X	L
	X	L	L
X	L	H	Z
Open	H	X	H
	X	L	H

H = high level, L = low level, X = irrelevant, ? = indeterminate, Z = high impedance (off)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

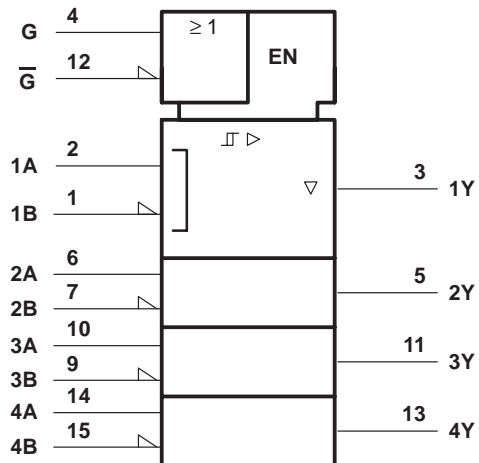
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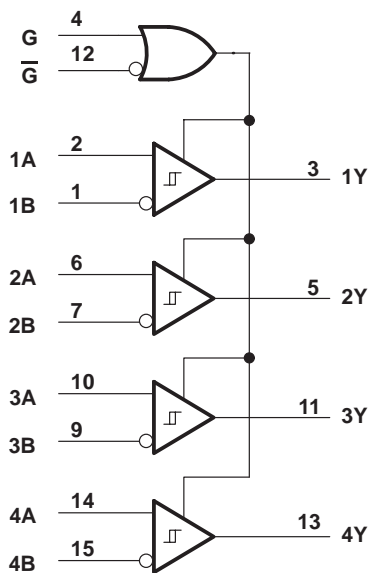
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logic symbol†

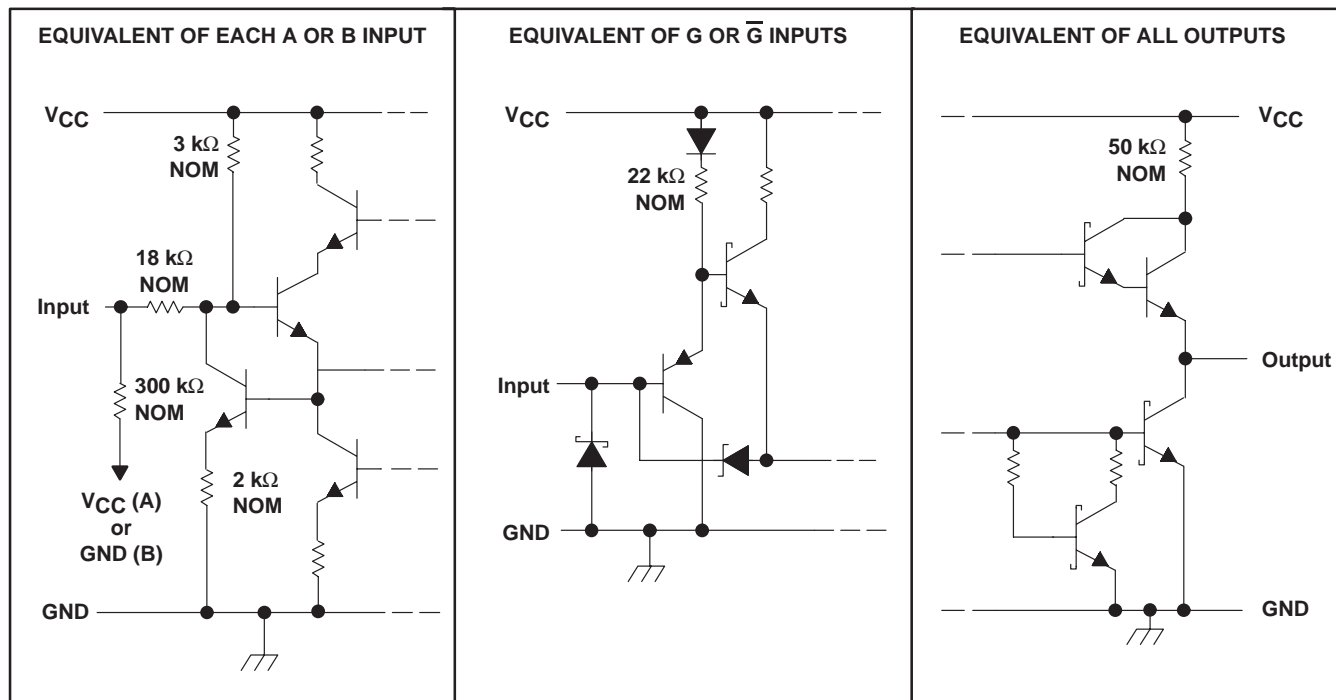


logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

schematics of inputs and outputs



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage, V_I (A or B inputs)	± 15 V
Differential input voltage, V_{ID} (see Note 2)	± 15 V
Enable input voltage, V_I	7 V
Low-level output current, I_{OL}	50 mA
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR	$T_A = 70^\circ\text{C}$ POWER RATING
D	950 mW	7.6 mW/ $^\circ\text{C}$	608 mW
N	1150 mW	9.2 mW/ $^\circ\text{C}$	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			± 7	V
Differential input voltage, V_{ID}			± 12	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			-400	μA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	$^\circ\text{C}$

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QUADRUPLE DIFFERENTIAL LINE RECEIVER

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electrical characteristics over recommended range of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V _{IT+}	Positive-going input threshold voltage				300	mV
V _{IT-}	Negative-going input threshold voltage		-300‡			mV
V _{hys}	Hysteresis voltage (V _{IT+} - V _{IT-})	See Figure 4		120		mV
V _{IK}	Enable-input clamp voltage	I _I = -18 mA			-1.5	V
V _{OH}	High-level output voltage	V _{ID} = 300 mV, I _{OH} = -400 μA	2.7	3.6		V
V _{OL}	Low-level output voltage	V _{ID} = -300 mV			0.45	V
			I _{OL} = 8 mA		0.5	
I _{OZ}	High-impedance-state output current	V _{CC} = 5.25 V	V _O = 2.4 V		20	μA
			V _{OH} = 0.4 V		-20	
I _I	Line input current	Other input at 0 V, See Note 3	V _I = 15 V		0.7	mA
			V _I = -15 V		-1.0	
I _H	High-level enable-input current			20	μA	
		V _{IH} = 5.25 V		100		
I _{IL}	Low-level enable-input current	V _{IL} = 0.4 V			-100	μA
	Input resistance		12	18		kΩ
I _{OS}	Short-circuit output current§	V _{ID} = 3 V, V _O = 0	-15	-78	-130	mA
I _{CC}	Supply current	Outputs disabled		22	35	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The algebraic convention, in which the less positive limit is designated minimum, is used in this data sheet for threshold voltage levels only.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 3: Refer to ANSI Standard EIA/TIA-422-B and EIA/TIA-423-B for exact conditions.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	Propagation delay time, low- to high-level output	V _{ID} = -2.5 V to 2.5 V, C _L = 15 pF, See Figure 2		15	22	ns
t _{PHL}	Propagation delay time, high- to low-level output			15	22	ns
t _{PZH}	Output enable time to high level	C _L = 15 pF, See Figure 3		13	25	ns
t _{PZL}	Output enable time to low level			11	25	
t _{PHZ}	Output disable time from high level	C _L = 15 pF, See Figure 3		13	25	ns
t _{PLZ}	Output disable time from low level			15	22	



PARAMETER MEASUREMENT INFORMATION

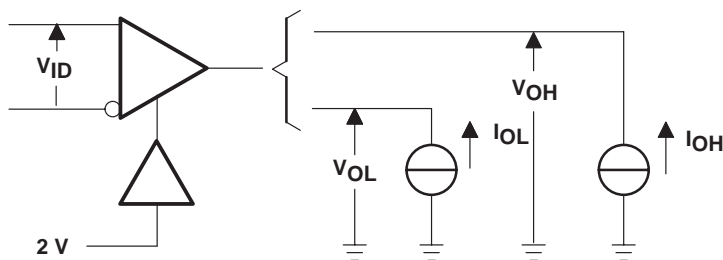
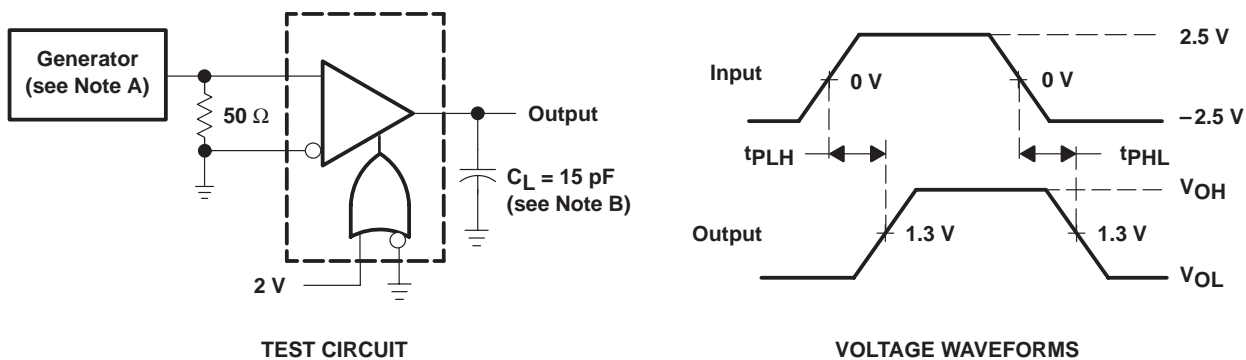


Figure 1. V_{OH} and V_{OL} Test Circuit



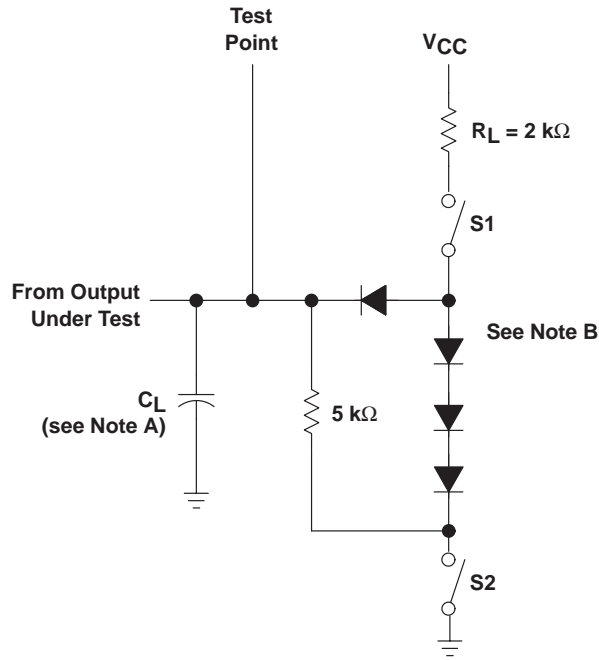
- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, duty cycle $\leq 50\%$, $Z_O = 50 \Omega$, $t_r \leq 6$ ns, $t_f \leq 6$ ns.
 B. C_L includes probe and jig capacitance.

Figure 2. t_{PLH} and t_{PHL} Test Circuit and Voltage Waveforms

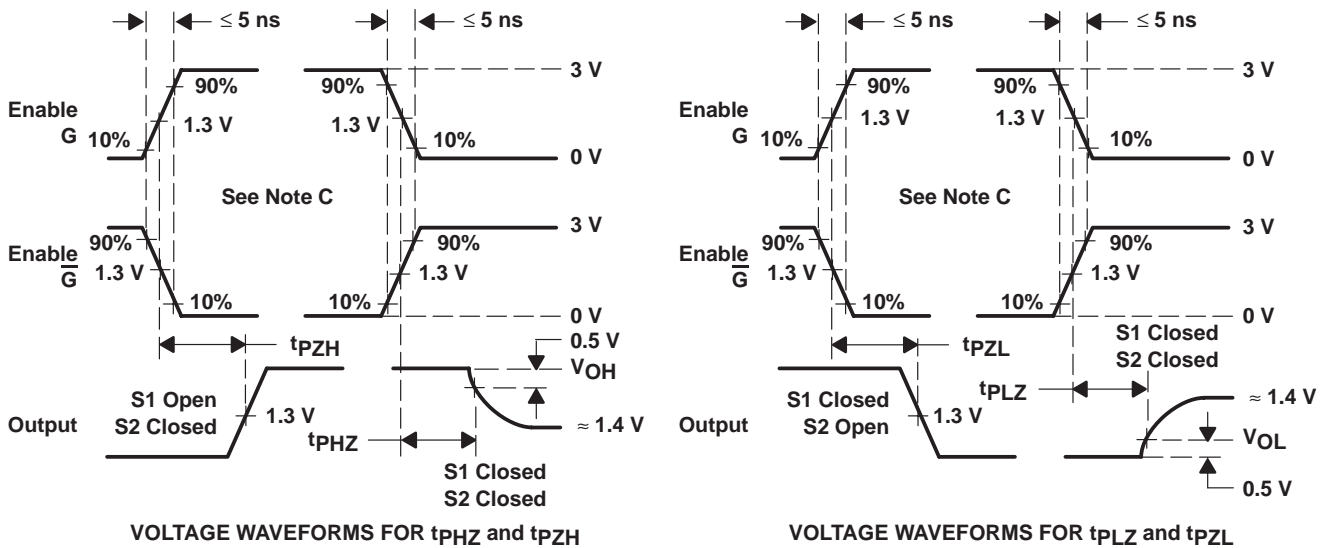
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PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



- NOTES: A. C_L includes probe and jig capacitance.
 B. All diodes are 1N3064 or equivalent.
 C. Enable G is tested with G high; \bar{G} is tested with G low.

Figure 3. t_{pZH} , t_{pZH} , t_{pLZ} , and t_{pZL} Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
 vs
 ENABLE VOLTAGE

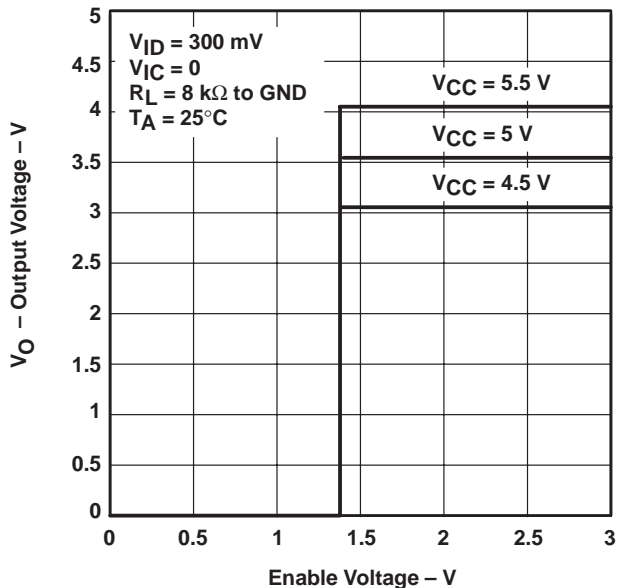


Figure 4

OUTPUT VOLTAGE
 vs
 ENABLE VOLTAGE

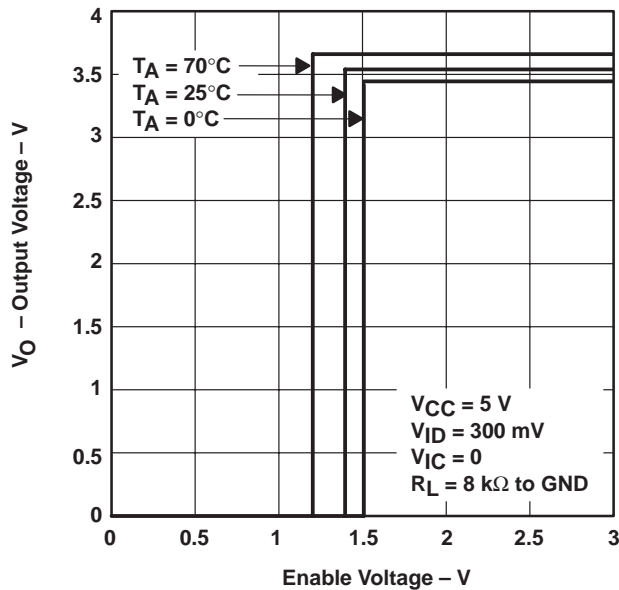


Figure 5

OUTPUT VOLTAGE
 vs
 ENABLE VOLTAGE

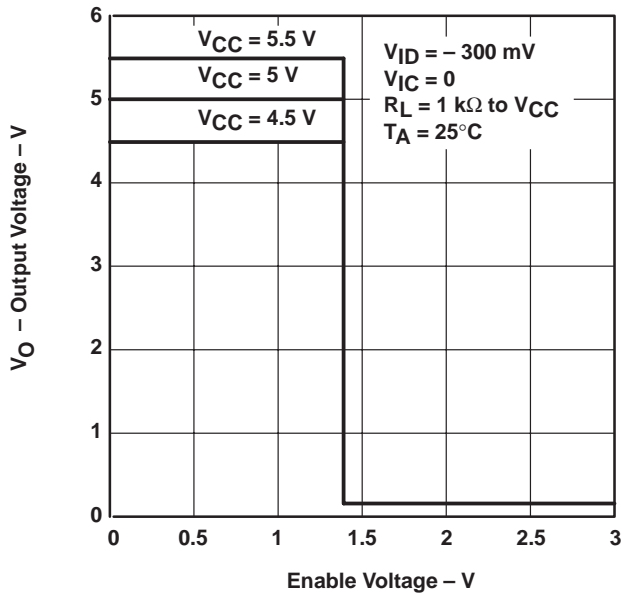


Figure 6

OUTPUT VOLTAGE
 vs
 ENABLE VOLTAGE

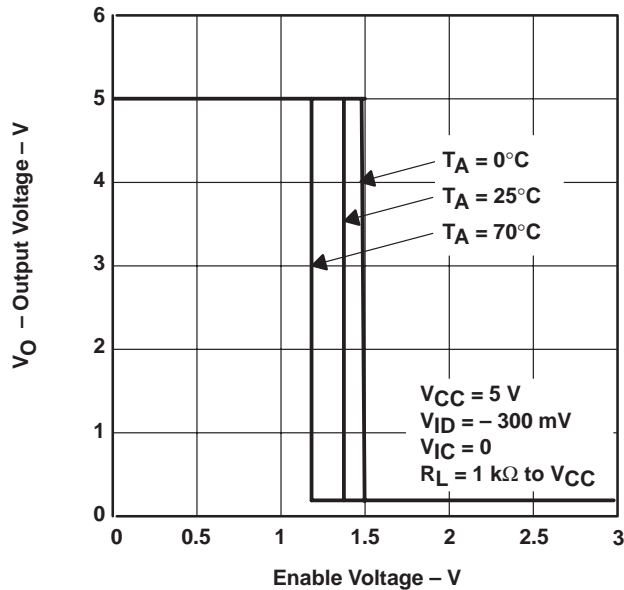
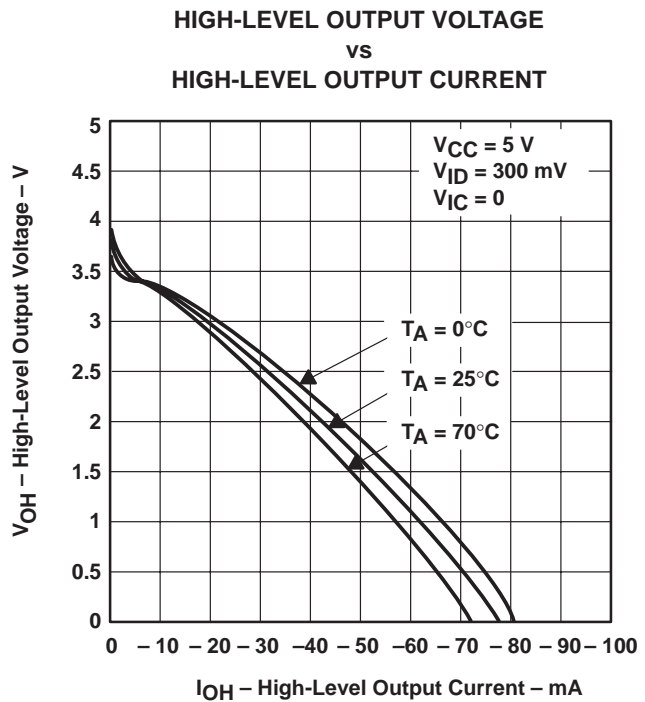
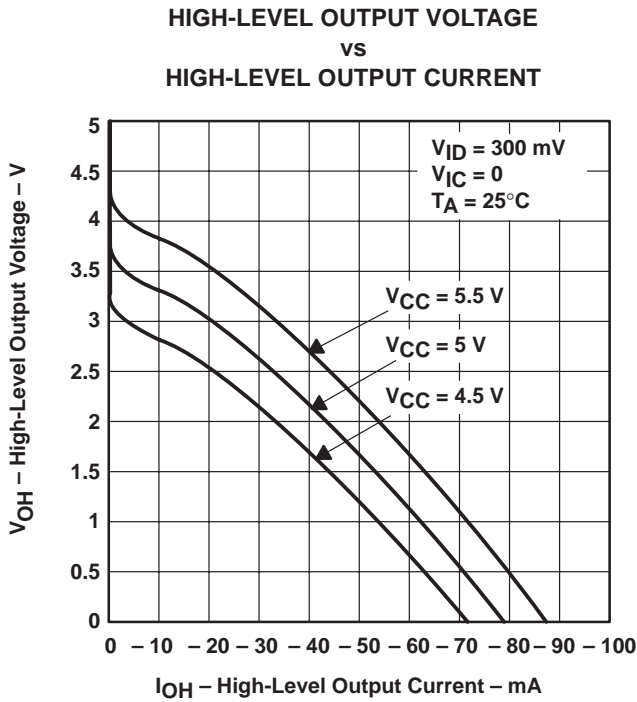
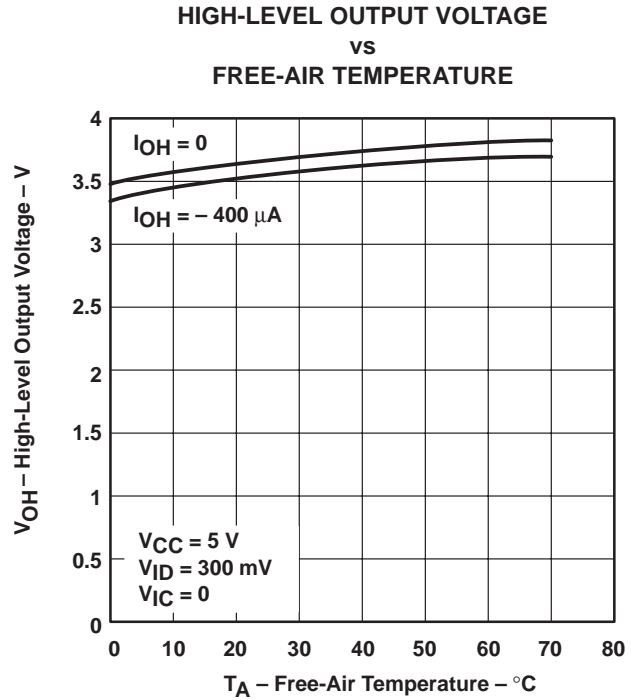
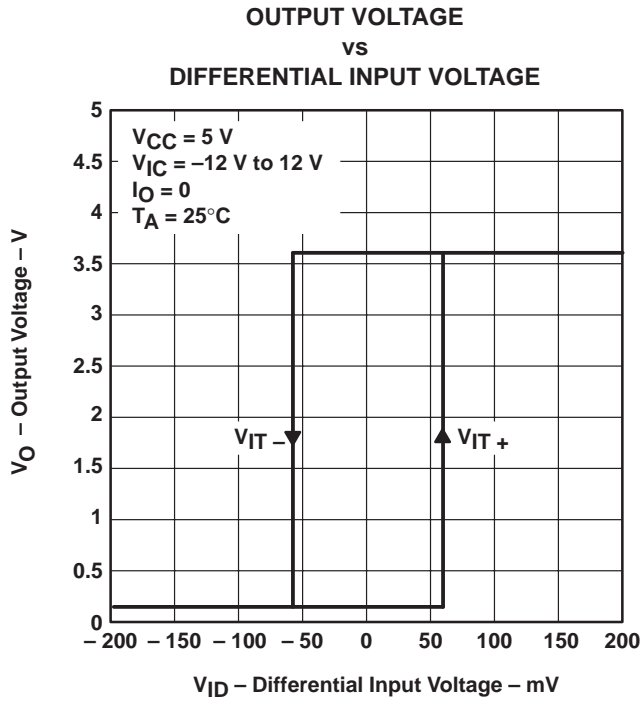


Figure 7

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TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
 vs
 FREE-AIR TEMPERATURE

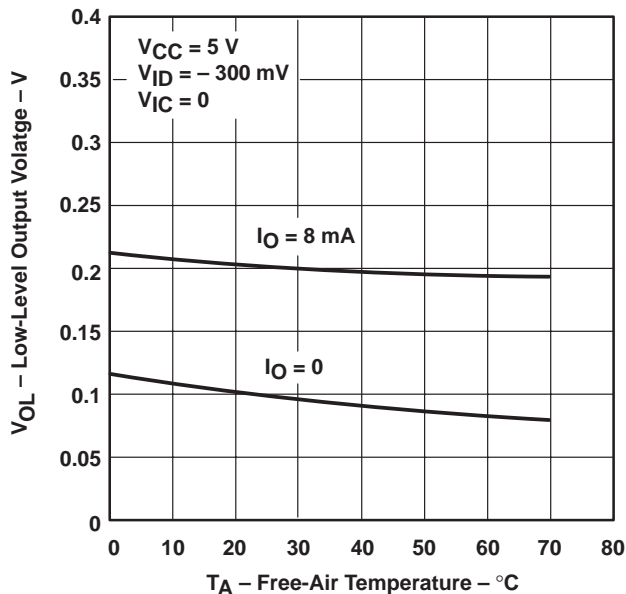


Figure 12

LOW-LEVEL OUTPUT VOLTAGE
 vs
 LOW-LEVEL OUTPUT CURRENT

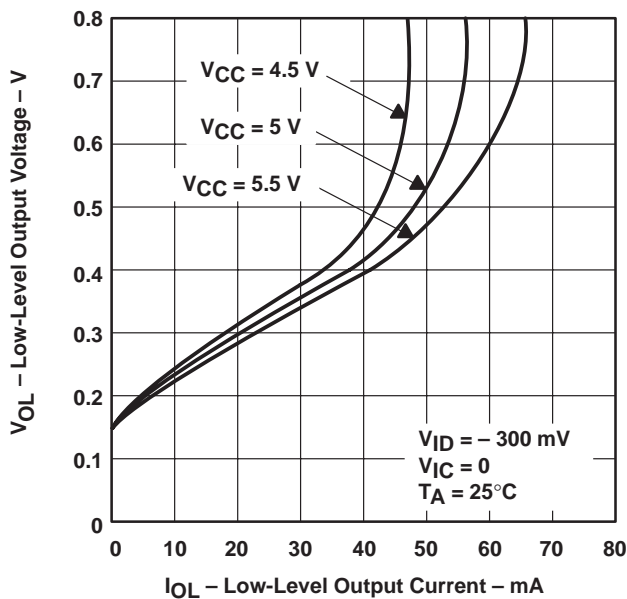


Figure 13

LOW-LEVEL OUTPUT VOLTAGE
 vs
 LOW-LEVEL OUTPUT CURRENT

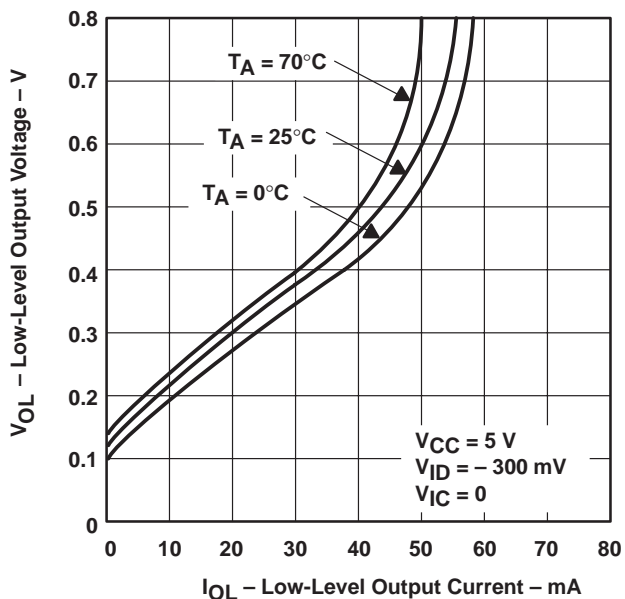
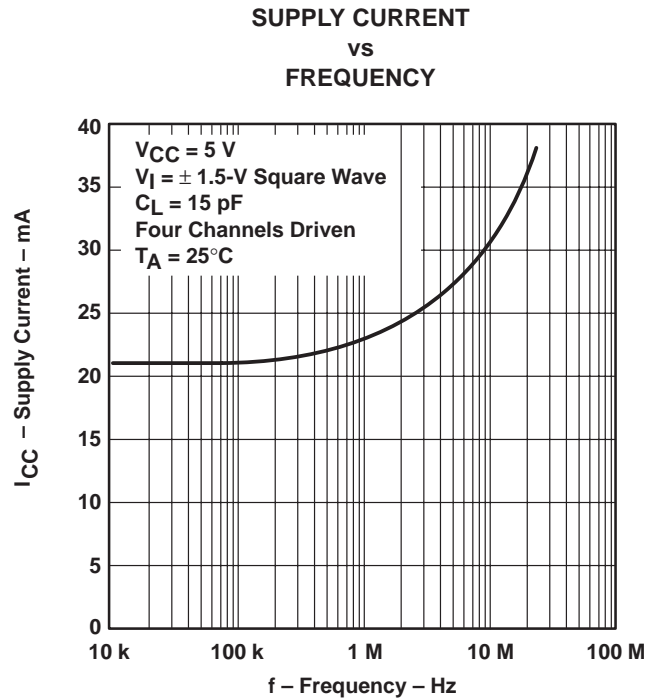
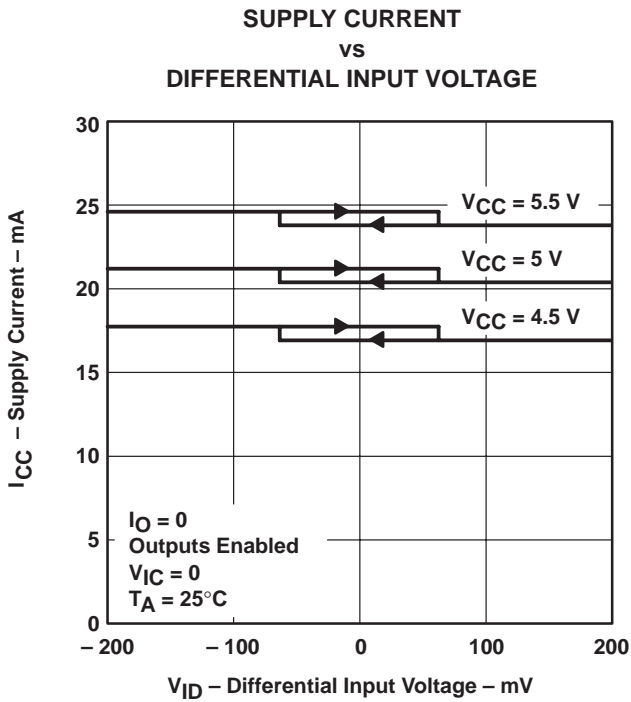
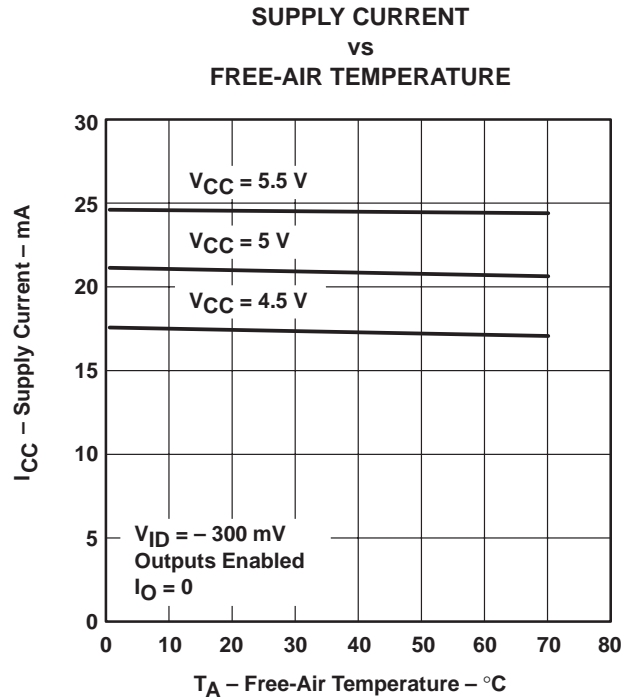
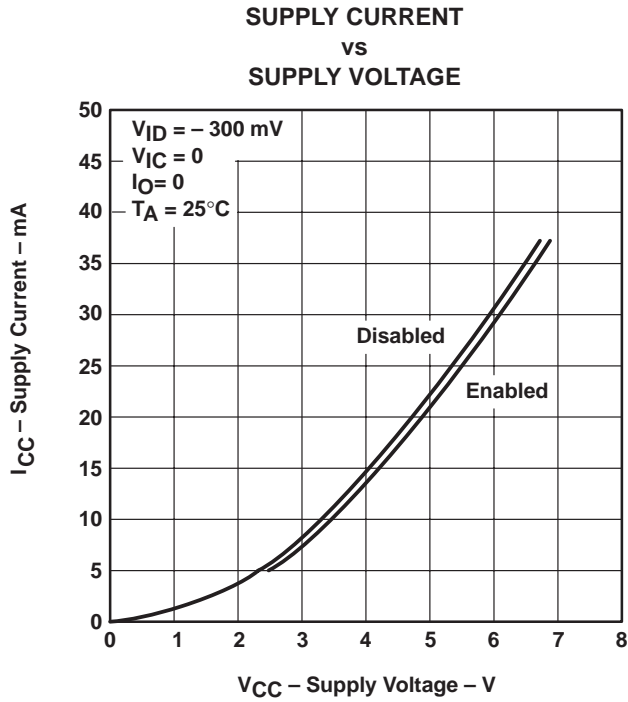


Figure 14

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TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

INPUT RESISTANCE
 vs
 FREE-AIR TEMPERATURE

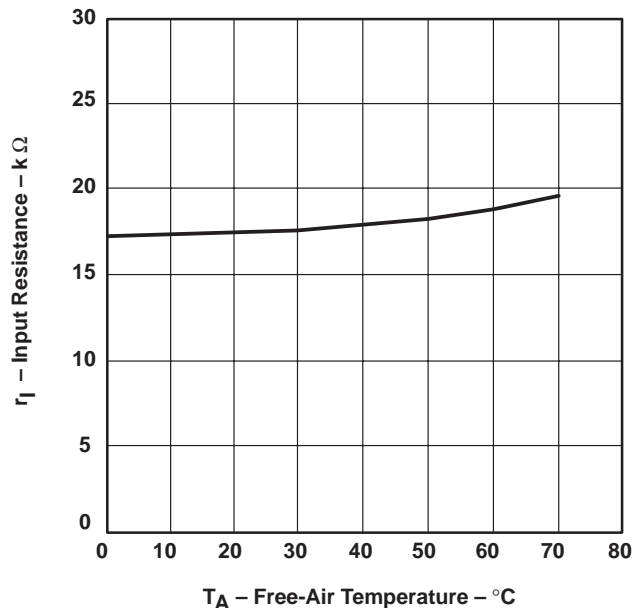


Figure 19

INPUT CURRENT
 vs
 INPUT VOLTAGE TO GND

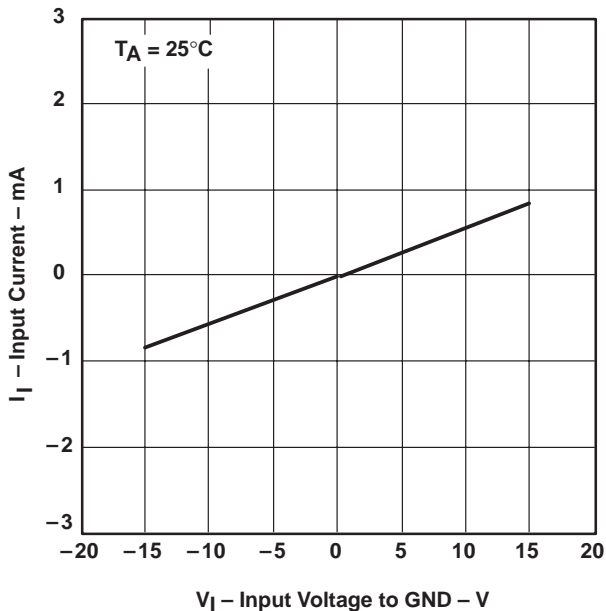


Figure 20

SWITCHING TIME
 vs
 FREE-AIR TEMPERATURE

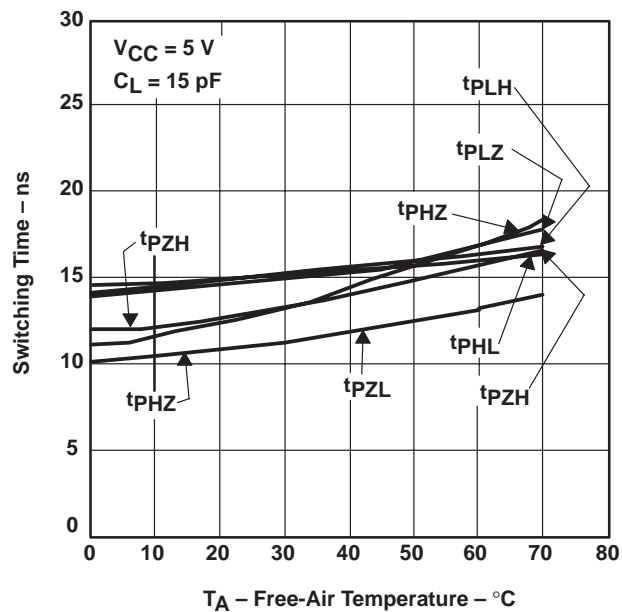


Figure 21

PROPAGATION DELAY TIME
 vs
 SUPPLY VOLTAGE

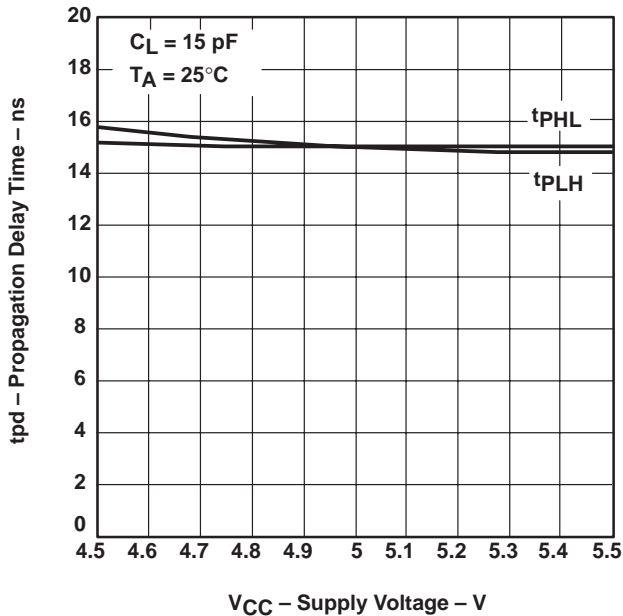


Figure 22

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