

# SN54ALS541, SN74ALS540, SN74ALS541 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

SDAS025D – APRIL 1982 – REVISED MARCH 2002

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- pnp Inputs Reduce dc Loading
- Data Flowthrough Pinout (All Inputs on Opposite Side From Outputs)

## description

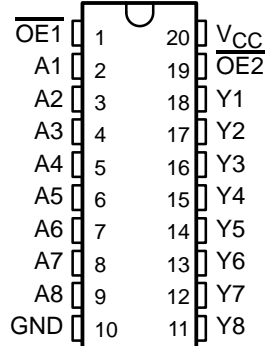
These octal buffers and line drivers are designed to have the performance of the popular SN54ALS240A/SN74ALS240A series and, at the same time, offer a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly facilitates printed circuit board layout.

The 3-state control gate is a 2-input NOR gate such that, if either output-enable ( $\overline{OE1}$  or  $\overline{OE2}$ ) input is high, all eight outputs are in the high-impedance state.

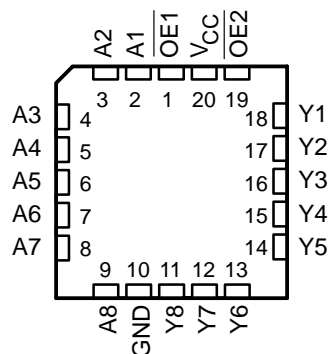
The SN74ALS540 provides inverted data. The 'ALS541 provide true data at the outputs.

The -1 versions of SN74ALS540 and SN74ALS541 are identical to the standard versions, except that the recommended maximum  $I_{OL}$  is increased to 48 mA. There is no -1 version of the SN54ALS541.

SN54ALS541 . . . J PACKAGE  
SN74ALS540 . . . DW, N, OR NS PACKAGE  
SN74ALS541 . . . DB, DW, N, OR NS PACKAGE  
(TOP VIEW)



SN54ALS541 . . . FK PACKAGE  
(TOP VIEW)



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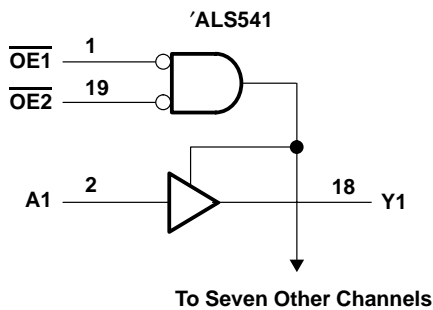
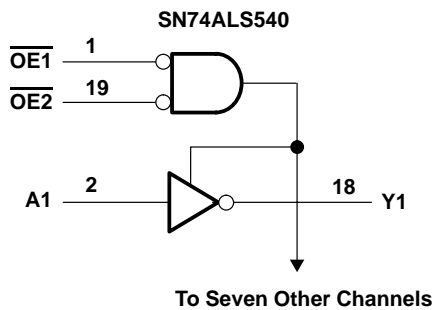
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## ORDERING INFORMATION

T <sub>A</sub>	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74ALS540N	SN74ALS540N
			SN74ALS540-1N	SN74ALS540-1N
			SN74ALS541N	SN74ALS541N
			SN74ALS541-1N	SN74ALS541-1N
	SOIC – DW	Tube	SN74ALS540DW	ALS540
		Tape and reel	SN74ALS540DWR	
		Tube	SN74ALS540-1DW	ALS540-1
		Tube	SN74ALS541DW	
		Tape and reel	SN74ALS541DWR	ALS541
		Tube	SN74ALS541-1DW	
	SOP – NS	Tape and reel	SN74ALS540NSR	ALS540
			SN74ALS540-1NSR	ALS540-1
			SN74ALS541NSR	ALS541
	SSOP – DB	Tape and reel	SN74ALS541DBR	G541
SN74ALS541-1DBR			G541-1	
–55°C to 125°C	CDIP – J	Tube	SNJ54ALS541J	SNJ54ALS541J
	LCCC – FK	Tube	SNJ54ALS541FK	SNJ54ALS541FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

## logic diagrams (positive logic)



# SN54ALS541, SN74ALS540, SN74ALS541 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

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## absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, $V_{CC}$ .....	7 V	
Input voltage, $V_I$ .....	7 V	
Voltage applied to a disabled 3-state output .....	5.5 V	
Package thermal impedance, $\theta_{JA}$ (see Note 1):	DB package .....	70°C/W
	DW package .....	58°C/W
	N package .....	69°C/W
	NS package .....	60°C/W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C	

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions

	SN54ALS541			SN74ALS540 SN74ALS541			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$ Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$ High-level input voltage	2			2			V
$V_{IL}$ Low-level input voltage			0.7			0.8	V
$I_{OH}$ High-level output current			–12			–15	mA
$I_{OL}$ Low-level output current			12			24	mA
						48†	
$T_A$ Operating free-air temperature	–55		125	0		70	°C

† Applies only to the -1 version and only if  $V_{CC}$  is between 4.75 V and 5.25 V



# SN54ALS541, SN74ALS540, SN74ALS541

## OCTAL BUFFERS AND LINE DRIVERS

### WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS541			SN74ALS540 SN74ALS541			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA		-1.2			-1.2			V
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V to 5.5 V, I <sub>OH</sub> = -0.4 mA		V <sub>CC</sub> - 2			V <sub>CC</sub> - 2			V
	V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = -3 mA	2.4	3.2	2.4	3.2			
		I <sub>OH</sub> = -12 mA	2		2				
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 12 mA	0.25 0.4		0.25 0.4				
		I <sub>OL</sub> = 24 mA			0.35 0.5				
		I <sub>OL</sub> = 48 mA†			0.35 0.5				
I <sub>OZH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V	20			20			μA	
I <sub>OZL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.4 V	-20			-20			μA	
I <sub>I</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 7 V	0.1			0.1			mA	
I <sub>IH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 2.7 V	20			20			μA	
I <sub>IL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0.4 V	-0.2			-0.1			mA	
I <sub>O§</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.25 V	-20	-112		-30	-112		mA	
I <sub>CC</sub>	SN74ALS540	V <sub>CC</sub> = 5.5 V	Outputs high		5 10			mA	
			Outputs low		13 22				
			Outputs disabled		11 19				
	ALS541	V <sub>CC</sub> = 5.5 V	Outputs high		6	14			
			Outputs low		15	25			
			Outputs disabled		13.5	32			

† Applies only to the -1 version and only if V<sub>CC</sub> is between 4.75 V and 5.25 V

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I<sub>O§</sub>.

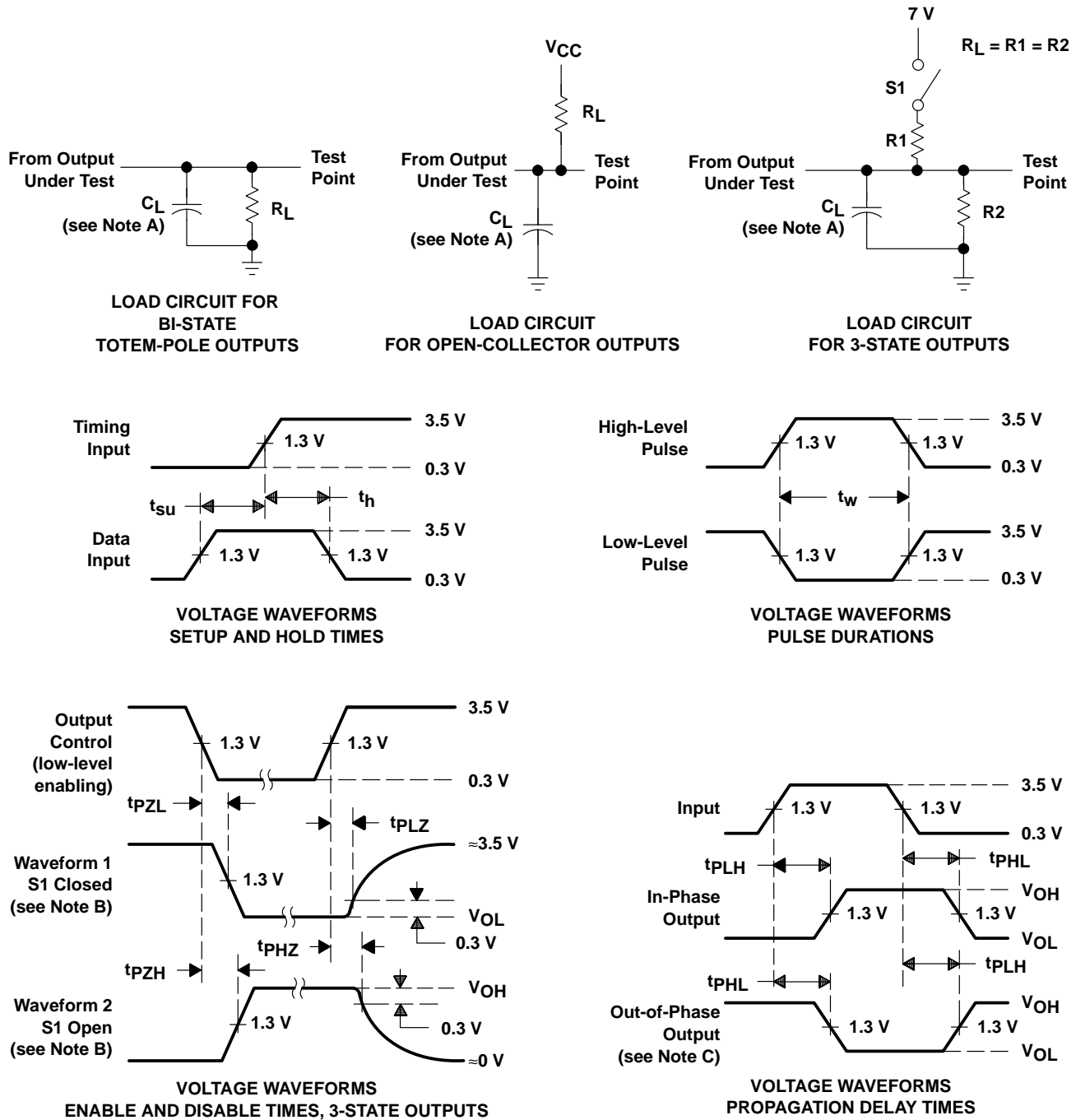
### switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>1</sub> = 500 Ω, R <sub>2</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX†						UNIT
			SN54ALS541		SN74ALS540		SN74ALS541		
			MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A	Y	4	17	2	12	4	14	ns
t <sub>PHL</sub>			2	14	2	9	2	10	
t <sub>PZH</sub>	OE	Y	5	18	5	15	5	15	ns
t <sub>PZL</sub>			8	28	8	20	8	20	
t <sub>PHZ</sub>	OE	Y	1	12	1	10	1	10	ns
t <sub>PLZ</sub>			2	14	2	12	2	12	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



PARAMETER MEASUREMENT INFORMATION  
 SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

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