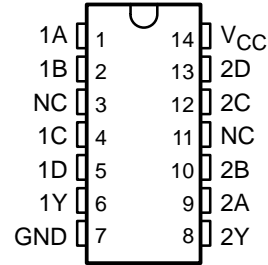


CD54ACT20, CD74ACT20 DUAL 4-INPUT POSITIVE-NAND GATES

SCHS320 – NOVEMBER 2002

- Inputs Are TTL-Voltage Compatible
- Speed of Bipolar F, AS, and S, With Significantly Reduced Power Consumption
- Balanced Propagation Delays
- ± 24 -mA Output Drive Current
– Fanout to 15 F Devices
- SCR-Latchup-Resistant CMOS Process and Circuit Design
- Exceeds 2-kV ESD Protection Per MIL-STD-883, Method 3015

CD54ACT20 . . . F PACKAGE
CD74ACT20 . . . E OR M PACKAGE
(TOP VIEW)



description/ordering information

The 'ACT20 devices contain two independent 4-input NAND gates. They perform the Boolean function $Y = \overline{A \cdot B \cdot C \cdot D}$ or $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$ in positive logic.

ORDERING INFORMATION

| T _A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|----------|---------------|-----------------------|------------------|
| –55°C to 125°C | PDIP – E | Tube | CD74ACT20E | CD74ACT20E |
| | SOIC – M | Tube | CD74ACT20M | ACT20M |
| | | Tape and reel | CD74ACT20M96 | |
| | CDIP – F | Tube | CD54ACT20F3A | CD54ACT20F3A |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (each gate)

| INPUTS | | | | OUTPUT Y |
|--------|---|---|---|-------------|
| A | B | C | D | |
| H | H | H | H | L |
| L | X | X | X | H |
| X | L | X | X | H |
| X | X | L | X | H |
| X | X | X | L | H |

logic diagram (positive logic)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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CD54ACT20, CD74ACT20 DUAL 4-INPUT POSITIVE-NAND GATES

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absolute maximum ratings over operating free-air temperature range†

| | |
|---|----------------|
| Supply voltage range, V_{CC} | -0.5 V to 6 V |
| Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) | ± 20 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) | ± 50 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | ± 50 mA |
| Continuous current through V_{CC} or GND | ± 100 mA |
| Package thermal impedance, θ_{JA} (see Note 2): E package | 80°C/W |
| M package | 86°C/W |
| Storage temperature range, T_{stg} | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

| | $T_A = 25^\circ\text{C}$ | | $-55^\circ\text{C to } 125^\circ\text{C}$ | | $-40^\circ\text{C to } 85^\circ\text{C}$ | | UNIT |
|--|--------------------------|----------|---|----------|--|----------|------|
| | MIN | MAX | MIN | MAX | MIN | MAX | |
| V_{CC} Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | 4.5 | 5.5 | V |
| V_{IH} High-level input voltage | 2 | | 2 | | 2 | | V |
| V_{IL} Low-level input voltage | | 0.8 | | 0.8 | | 0.8 | V |
| V_I Input voltage | 0 | V_{CC} | 0 | V_{CC} | 0 | V_{CC} | V |
| V_O Output voltage | 0 | V_{CC} | 0 | V_{CC} | 0 | V_{CC} | V |
| I_{OH} High-level output current | | -24 | | -24 | | -24 | mA |
| I_{OL} Low-level output current | | 24 | | 24 | | 24 | mA |
| $\Delta t/\Delta v$ Input transition rise or fall rate | | 10 | | 10 | | 10 | ns/V |

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



CD54ACT20, CD74ACT20 DUAL 4-INPUT POSITIVE-NAND GATES

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | V _{CC} | T _A = 25°C | | –55°C to 125°C | | –40°C to 85°C | | UNIT |
|-------------------------------|---|---------------------------------------|-----------------|-----------------------|------|----------------|------|---------------|-----|------|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| V _{OH} | V _I = V _{IH} or V _{IL} | I _{OH} = –50 μA | 4.5 V | 4.4 | | 4.4 | | 4.4 | V | |
| | | I _{OH} = –24 mA | 4.5 V | 3.94 | | 3.7 | | 3.8 | | |
| | | I _{OH} = –50 mA [†] | 5.5 V | | | 3.85 | | | | |
| | | I _{OH} = –75 mA [†] | 5.5 V | | | | | 3.85 | | |
| V _{OL} | V _I = V _{IH} or V _{IL} | I _{OL} = 50 μA | 4.5 V | | 0.1 | | 0.1 | 0.1 | V | |
| | | I _{OL} = 24 mA | 4.5 V | | 0.36 | | 0.5 | 0.44 | | |
| | | I _{OL} = 50 mA [†] | 5.5 V | | | | 1.65 | | | |
| | | I _{OL} = 75 mA [†] | 5.5 V | | | | | 1.65 | | |
| I _I | V _I = V _{CC} or GND | | 5.5 V | | ±0.1 | | ±1 | ±1 | μA | |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | | 5.5 V | | 4 | | 80 | 40 | μA | |
| ΔI _{CC} [‡] | V _I = V _{CC} – 2.1 V | | 4.5 V to 5.5 V | | 2.4 | | 3 | 2.8 | mA | |
| C _i | | | | | 10 | | 10 | 10 | pF | |

[†] Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C.

[‡] Additional quiescent supply current per input pin, TTL inputs high, 1 unit load

ACT INPUT LOAD TABLE

| INPUT | UNIT LOAD |
|-------|-----------|
| All | 0.27 |

Unit Load is ΔI_{CC} limit specified in electrical characteristics table (e.g., 2.4 mA at 25°C).

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V, C_L = 50 pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | –55°C to 125°C | | –40°C to 85°C | | UNIT |
|------------------|---------------|-------------|----------------|------|---------------|------|------|
| | | | MIN | MAX | MIN | MAX | |
| t _{PLH} | A, B, C, or D | Y | 3.4 | 13.5 | 3.5 | 12.3 | ns |
| t _{PHL} | | | 3.4 | 13.5 | 3.5 | 12.3 | |

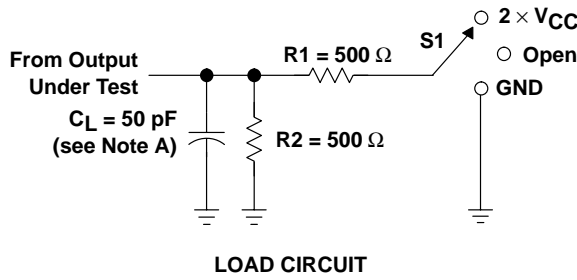
operating characteristics, T_A = 25°C

| PARAMETER | TYP | UNIT |
|---|-----|------|
| C _{pd} Power dissipation capacitance | 48 | pF |

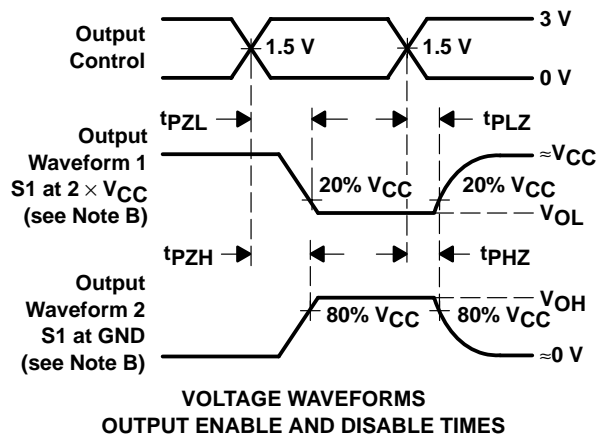
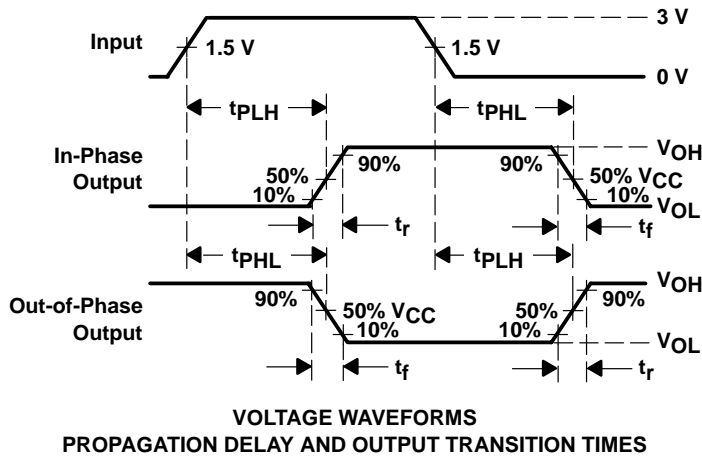
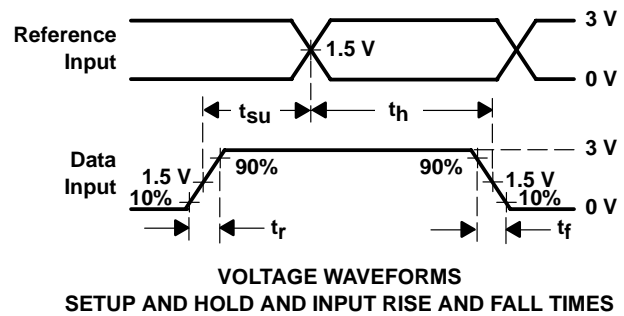
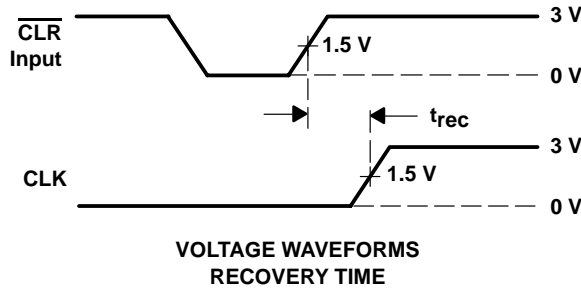
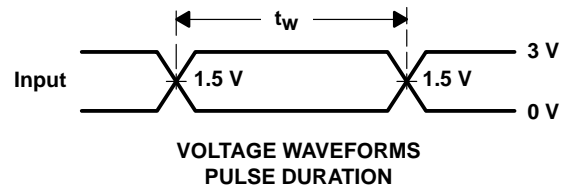
CD54ACT20, CD74ACT20 DUAL 4-INPUT POSITIVE-NAND GATES

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PARAMETER MEASUREMENT INFORMATION



| TEST | S1 |
|-------------------|-------------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | $2 \times V_{CC}$ |
| t_{PHZ}/t_{PZH} | GND |



- NOTES:
- C_L includes probe and test-fixture capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$. Phase relationships between waveforms are arbitrary.
 - For clock inputs, f_{max} is measured with the input duty cycle at 50%.
 - The outputs are measured one at a time with one input transition per measurement.
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .

Figure 1. Load Circuit and Voltage Waveforms

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012 variation AB.

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