

## FEATURES

- Both  $V_{CC}$  and VPP Switching in a Single Package
- Built-In Current Limit and Thermal Shutdown
- 16-Pin (Narrow) SOIC Package
- Inrush Current Limited (Drives 150 $\mu$ F Loads)
- Continuous 12V Power Not Required
- Extremely Low  $R_{DS(ON)}$  NMOS Switches
- Guaranteed 1A  $V_{CC}$  Current and 120mA VPP Current
- 1 $\mu$ A Quiescent Current in Standby
- No External Components Required
- Compatible with Industry Standard Controllers
- Break-Before-Make Switching
- Controlled Rise and Fall Times

## APPLICATIONS

- Notebook Computers
- Palmtop Computers
- Pen-Based Computers
- Handi-Terminals
- Bar-Code Readers

## DESCRIPTION

The LTC<sup>®</sup>1472 switching matrix routes power to both the  $V_{CC}$  and VPP power supply pins of the PCMCIA compatible card socket. The  $V_{CC}$  output of the LTC1472 is switched between three operating states: OFF, 3.3V, and 5V. The VPP output is switched between four operating states: 0V,  $V_{CC}$ , 12V, and Hi-Z. The output voltages are selected by two sets of digital inputs which are compatible with industry standard PC Card controllers (see Truth Tables).

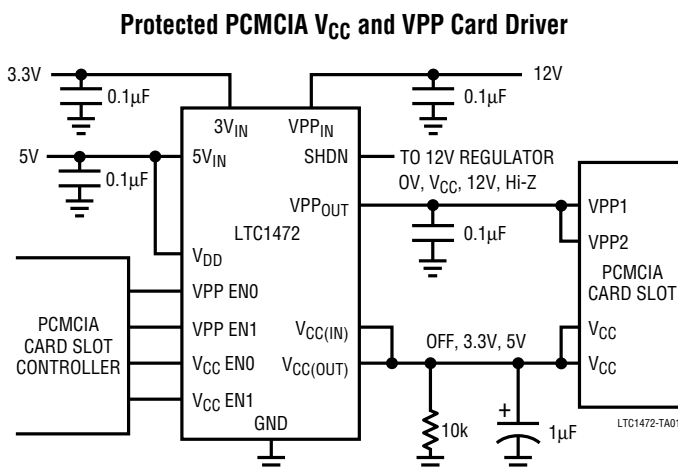
The  $V_{CC}$  output of the LTC1472 can supply up to 1A of current and the VPP output up to 120mA. Both switches have built-in SafeSlot<sup>™</sup> current limiting and thermal shutdown to protect the card, socket and power supply against accidental short-circuit conditions.

The LTC1472 is designed to conserve power by automatically dropping to 1 $\mu$ A standby current when the two outputs are switched OFF. A shutdown pin is provided which holds the external 12V regulator in standby mode except when required for VPP power.

The LTC1472 is available in 16-pin SO.

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 SafeSlot is a trademark of Linear Technology Corporation.

## TYPICAL APPLICATION



### Linear Technology PCMCIA Product Family

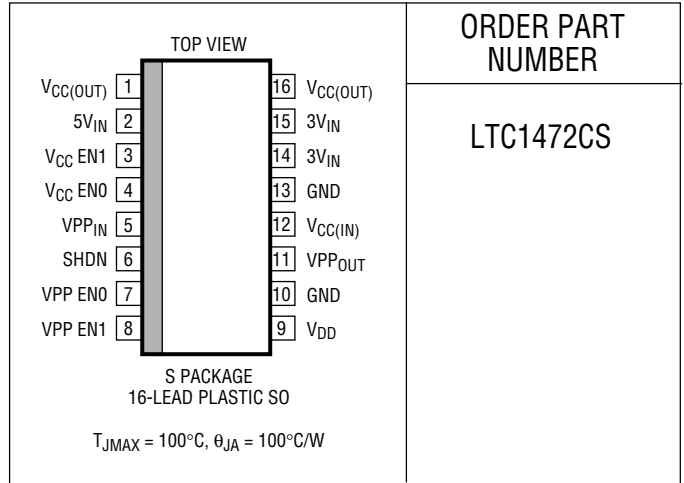
DEVICE	DESCRIPTION	PACKAGE
LT <sup>®</sup> 1312	Single PCMCIA VPP Driver/Regulator	8-Pin SO
LT1313	Dual PCMCIA VPP Driver/Regulator	16-Pin SO*
LTC1314	Single PCMCIA Switch Matrix	14-Pin SO
LTC1315	Dual PCMCIA Switch Matrix	24-Pin SSOP
LTC1470	Protected $V_{CC}$ 5V/3.3V Switch Matrix	8-Pin SO
LTC1471	Dual Protected $V_{CC}$ 5V/3.3V Switch Matrix	16-Pin SO*
LTC1472	Protected $V_{CC}$ and VPP Switch Matrix	16-Pin SO*

\*Narrow Body

**ABSOLUTE MAXIMUM RATINGS**

5V <sub>IN</sub> Supply Voltage .....	-0.3V to 7V
3V <sub>IN</sub> Supply Voltage .....	-0.3V to 7V
VPP <sub>IN</sub> Supply Voltage .....	-0.3V to 13.2V
V <sub>CC(IN)</sub> Supply Voltage .....	-0.3 to 7V
V <sub>DD(IN)</sub> Supply Voltage .....	-0.3V to 7V
VPP <sub>OUT</sub> (OFF) .....	-0.3V to 13.2V
V <sub>CC(OUT)</sub> (OFF) .....	-0.3V to 7V
Enable Inputs .....	-0.3V to 7V
VPP <sub>OUT</sub> Short-Circuit Duration .....	Indefinite
V <sub>CC(OUT)</sub> Short-Circuit Duration .....	Indefinite
Operating Temperature Range .....	0°C to 70°C
Junction Temperature .....	100°C
Storage Temperature Range .....	-65°C to 150°C
Lead Temperature (Soldering, 10 sec).....	300°C

**PACKAGE/ORDER INFORMATION**



Consult factory for Industrial and Military grade parts.

**ELECTRICAL CHARACTERISTICS** (V<sub>CC</sub> Switch Section)

5V<sub>IN</sub> = 5V, 3V<sub>IN</sub> = 3.3V, VPP EN0 = VPP EN1 = 0V, T<sub>A</sub> = 25°C, (Note 1) unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
5V <sub>IN</sub>	5V <sub>IN</sub> Supply Voltage Range	(Note 2)	4.75		5.25	V	
3V <sub>IN</sub>	3V <sub>IN</sub> Supply Voltage Range	(Note 3)	0		3.60	V	
I <sub>5VIN</sub>	5V <sub>IN</sub> Supply Current	Program to Hi-Z Program to 5V, No Load Program to 3.3V, No Load	●	0.01 140 100	10 200 160	μA	
I <sub>3VIN</sub>	3V <sub>IN</sub> Supply Current	Program to Hi-Z. Program to 5V, No Load Program to 3.3V, No Load	●	0.01 0.01 40	10 10 80	μA	
R <sub>ON</sub>	5V Switch On Resistance 3.3V Switch On Resistance	Program to 5V, I <sub>OUT</sub> = 500mA Program to 3.3V, I <sub>OUT</sub> = 500mA		0.14 0.12	0.18 0.16	Ω	
I <sub>LKG</sub>	Output Leakage Current OFF	V <sub>CC</sub> EN0 = V <sub>CC</sub> EN1 = 0V or 5V, 0V ≤ V <sub>CC(OUT)</sub> ≤ 5V	●		±10	μA	
I <sub>LIM5V</sub>	V <sub>CC(OUT)</sub> 5V Current Limit	Program to 5V, V <sub>CC(OUT)</sub> = 0V (Note 4)		1		A	
I <sub>LIM3V</sub>	V <sub>CC(OUT)</sub> 3.3V Current Limit	Program to 3.3V, V <sub>CC(OUT)</sub> = 0V (Note 4)		1		A	
V <sub>CCENH</sub>	V <sub>CC</sub> Enable Input High Voltage		●	2		V	
V <sub>CCENL</sub>	V <sub>CC</sub> Enable Input Low Voltage		●		0.8	V	
I <sub>VCCEN</sub>	V <sub>CC</sub> Enable Input Current	0V ≤ V <sub>CCEN</sub> ≤ 5V	●		±1	μA	
t <sub>VCC1</sub>	Delay + Rise Time	From 0V to 3.3V, R <sub>LOAD</sub> = 100Ω, C <sub>LOAD</sub> = 1μF (Note 5)		0.2	0.32	1	ms
t <sub>VCC2</sub>	Delay + Rise Time	From 3.3V to 5V, R <sub>LOAD</sub> = 100Ω, C <sub>LOAD</sub> = 1μF (Note 5)		0.2	0.52	1	ms
t <sub>VCC3</sub>	Delay + Rise Time	From 0V to 5V, R <sub>LOAD</sub> = 100Ω, C <sub>LOAD</sub> = 1μF (Note 5)		0.2	0.38	1	ms

## ELECTRICAL CHARACTERISTICS (VPP Switch Section)

$V_{DD} = 5V$ ,  $V_{CC(IN)} = 5V$ ,  $V_{PP(IN)} = 12V$ ,  $V_{CCEN0} = V_{CCEN1} = 0V$ ,  $T_A = 25^\circ C$ , (Note 1), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
$V_{CC(IN)}$	$V_{CC}$ Input Voltage Range		●	3	5.5	V	
$V_{PP(IN)}$	VPP Input Voltage Range	(Note 6)	●	0	12.6	V	
$V_{DD}$	Logic Supply Voltage Range	(Note 7)	●	4.5	5.5	V	
$I_{CC(IN)}$	$V_{CC(IN)}$ Supply Current, No Load	Program to $V_{PP(IN)}$ or $V_{CC(IN)}$ $V_{PP(IN)} = 12V$ Program to 0V or Hi-Z	● ●	35 0.01	60 10	$\mu A$ $\mu A$	
$I_{PP(IN)}$	$V_{PP(IN)}$ Supply Current, No Load	Program to $V_{PP(IN)}$ or $V_{CC(IN)}$ Program to 0V or Hi-Z	● ●	40 0.01	80 10	$\mu A$ $\mu A$	
$I_{DD}$	$V_{DD}$ Supply Current, No Load	Program to $V_{PP(IN)}$ Program to $V_{CC(IN)}$ , $V_{PP(IN)} = 0V$ Program to $V_{CC(IN)}$ , $V_{PP(IN)} = 12V$ Program to 0V or Hi-Z	● ● ● ●	70 85 40 0.01	120 150 80 10	$\mu A$ $\mu A$ $\mu A$ $\mu A$	
$I_{VPP(OUT)}$	Hi-Z Output Leakage Current	Program to Hi-Z, $0V < V_{PP(OUT)} < 12V$	●	0.01	10	$\mu A$	
$R_{ON}$	On Resistance $V_{PP(OUT)}$ to $V_{PP(IN)}$ On Resistance $V_{PP(OUT)}$ to $V_{CC(IN)}$ On Resistance $V_{PP(OUT)}$ to GND	$V_{PP(IN)} = 12V$ , $I_{LOAD} = 120mA$ $V_{CC(IN)} = 5V$ , $I_{LOAD} = 5mA$ $V_{DD} = 5V$ , $I_{SINK} = 1mA$		0.50 1.70 100	1 5 250	$\Omega$ $\Omega$ $\Omega$	
$V_{PP(ENH)}$	VPP Enable Input High Voltage	$V_{DD} = 5V$	●	2		V	
$V_{PP(ENL)}$	VPP Enable Input Low Voltage	$V_{DD} = 5V$	●		0.8	V	
$I_{VPP(EN)}$	VPP Enable Input Current	$0V < V_{PP(EN)} < V_{DD}$	●		$\pm 1$	$\mu A$	
$V_{SDH}$	SHDN Output High Voltage	Program to 0V, $V_{CC(IN)}$ or Hi-Z, $I_{LOAD} = 400\mu A$	●	3.5		V	
$V_{SDL}$	SHDN Output Low Voltage	Program to $V_{PP(IN)}$ , $I_{SINK} = 400\mu A$	●		0.4	V	
$I_{LIM(VCC)}$	$V_{PP(OUT)}$ Current Limit, $V_{CC(IN)}$	Program to $V_{CC(IN)}$ , $V_{PP(OUT)} = 0V$ (Note 4)		60		mA	
$I_{LIM(VPP)}$	$V_{PP(OUT)}$ Current Limit, $V_{PP(IN)}$	Program to $V_{PP(IN)}$ , $V_{PP(OUT)} = 0V$ (Note 4)		100		mA	
$t_{VPP1}$	Delay and Rise Time	From 0V to $V_{CC(IN)}$ , $V_{PP(IN)} = 0V$ (Note 8)		5	15	50	$\mu s$
$t_{VPP2}$	Delay and Rise Time	From 0V to $V_{PP(IN)}$ (Note 8)		25	85	250	$\mu s$
$t_{VPP3}$	Delay and Rise Time	From $V_{CC(IN)}$ to $V_{PP(IN)}$ (Note 8)		30	100	300	$\mu s$
$t_{VPP4}$	Delay and Fall Time	From $V_{PP(IN)}$ to $V_{CC(IN)}$ (Note 9)		5	15	50	$\mu s$
$t_{VPP5}$	Delay and Fall Time	From $V_{PP(IN)}$ to 0V (Note 10)		10	35	100	$\mu s$
$t_{VPP6}$	Delay and Fall Time	From $V_{CC(IN)}$ to 0V, $V_{PP(IN)} = 0V$ (Note 10)		10	30	100	$\mu s$
$t_{VPP7}$	Output Turn-On Delay	From Hi-Z to $V_{CC(IN)}$ (Note 8)		5	15	50	$\mu s$
$t_{VPP8}$	Output Turn-On Delay	From Hi-Z to $V_{PP(IN)}$ (Note 8)		25	85	250	$\mu s$

The ● denotes the specifications which apply over the full operating temperature range.

**Note 1:**  $V_{ENH} = 5V$ ,  $V_{ENL} = 0V$ . See  $V_{CC}$  and VPP Switch Truth Tables for programming enable inputs for desired output states.

**Note 2:** Power for the  $V_{CC}$  input logic and charge pump circuitry is derived from the  $5V_{IN}$  power supply which must be continuously powered. 12V and 3.3V power is not required to control the NMOS  $V_{CC}$  switches. (See Applications Information.)

**Note 3:** The two  $3V_{IN}$  supply input pins (14 and 15) must be connected together and the two  $V_{CC(OUT)}$  output pins (1 and 16) must be connected together. The  $3V_{IN}$  supply pins do not need to be continuously powered and may drop to 0V when not required.

**Note 4:** The  $V_{CC}$  and VPP output are protected with foldback current limit which reduces the short-circuit (0V) currents below peak permissible current levels at higher output voltages.

**Note 5:** To 90% of final value.

**Note 6:** 12V power is only required when  $V_{PP(OUT)}$  is programmed to 12V. The external 12V regulator can be shutdown at all other times. Built-in charge pumps power the internal NMOS switches from the 5V  $V_{DD}$  supply when 12V is not present.

**Note 7:** Power for the VPP input logic and charge pump circuitry is derived from the  $V_{DD}$  power supply which must be continuously powered.

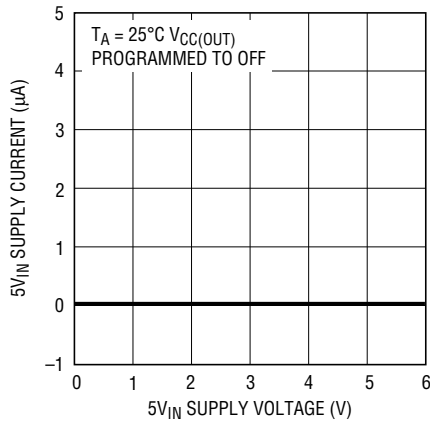
**Note 8:** To 90% of the final value,  $C_{OUT} = 0.1\mu F$ ,  $R_{OUT} = 2.9k$ .

**Note 9:** To 10% of the final value,  $C_{OUT} = 0.1\mu F$ ,  $R_{OUT} = 2.9k$ .

**Note 10:** To 50% of the initial value,  $C_{OUT} = 0.1\mu F$ ,  $R_{OUT} = 2.9k$ .

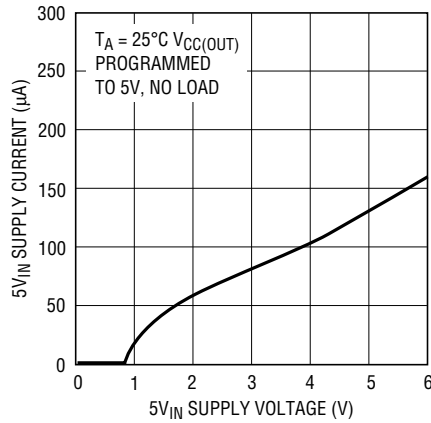
**TYPICAL PERFORMANCE CHARACTERISTICS** ( $V_{CC}$  Section)  $V_{PP\ EN0} = V_{PP\ EN1} = 0V$

**5V<sub>IN</sub> Supply Current (OFF)**



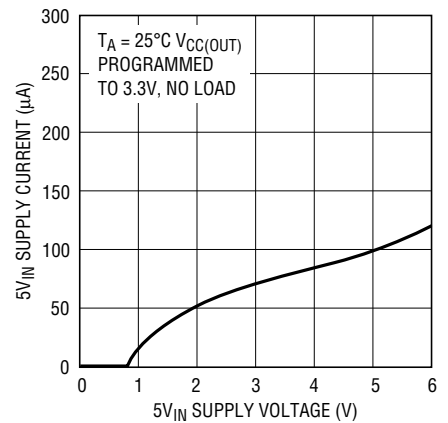
LTC1472 TPC01

**5V<sub>IN</sub> Supply Current (5V ON)**



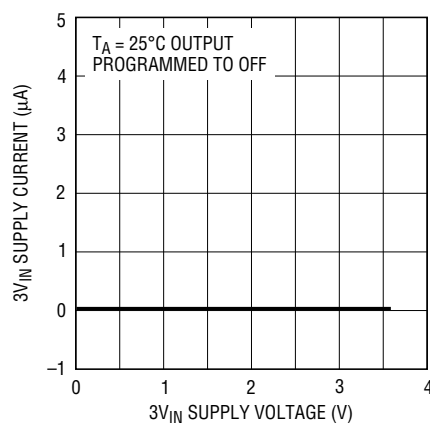
LTC1472 TPC02

**5V<sub>IN</sub> Supply Current (3.3V ON)**



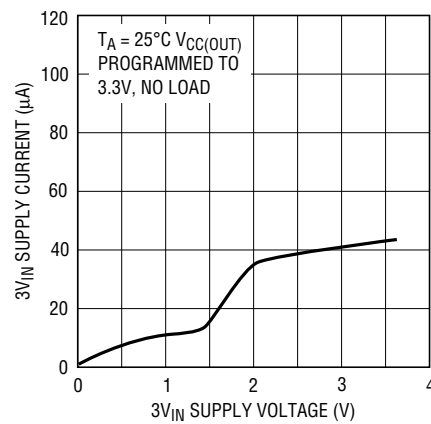
LTC1472 TPC03

**3V<sub>IN</sub> Supply Current (OFF)**



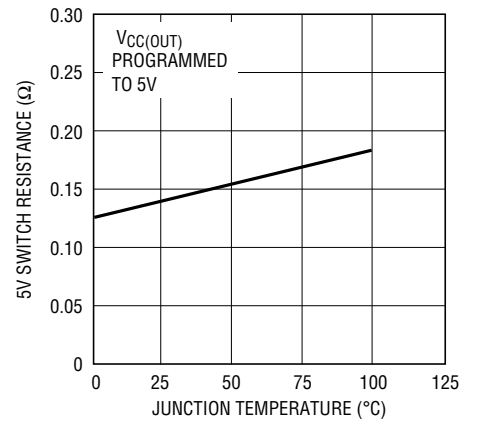
LTC1472 TPC04

**3V<sub>IN</sub> Supply Current (3.3V ON)**



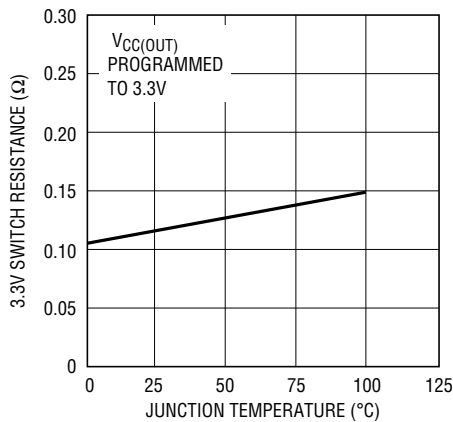
LTC1472 TPC05

**5V Switch Resistance**



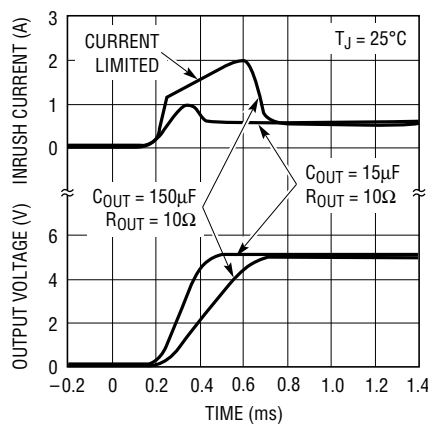
LTC1472 TPC06

**3.3V Switch Resistance**



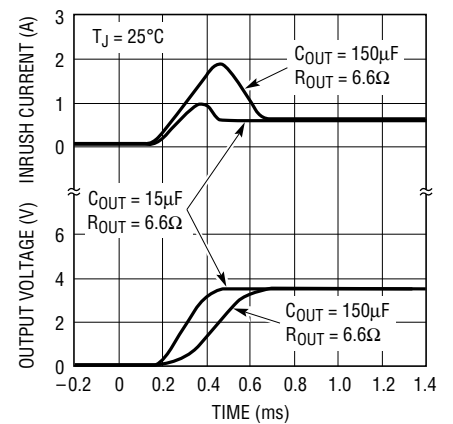
LTC1472 TPC07

**Inrush Current (5V Switch)**



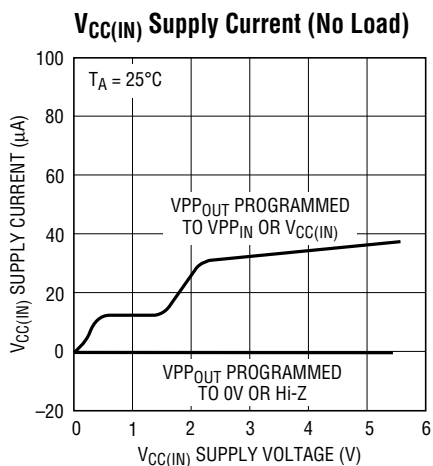
LTC1472 TPC08

**Inrush Current (3.3V Switch)**

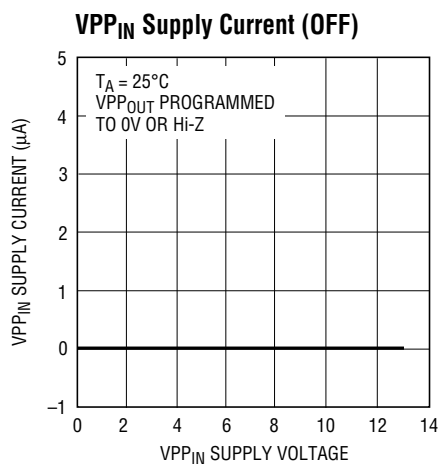


LTC1472 TPC09

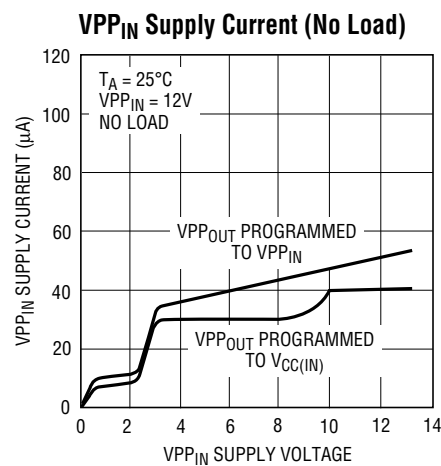
**TYPICAL PERFORMANCE CHARACTERISTICS** (VPP Section)  $V_{CC\ EN0} = V_{CC\ EN1} = 0V$



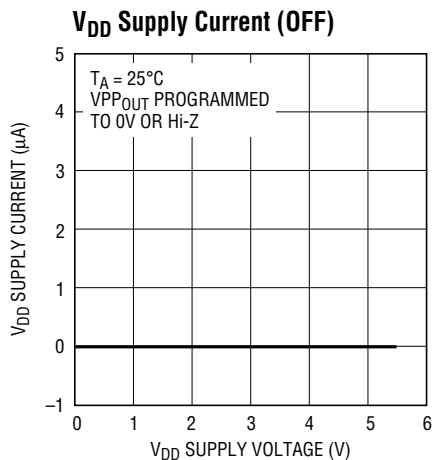
LTC1472 TPC10



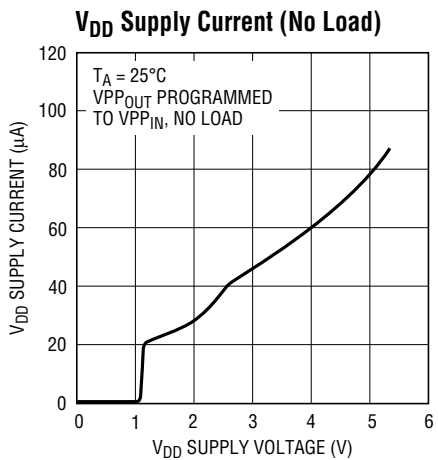
LTC1472 TPC11



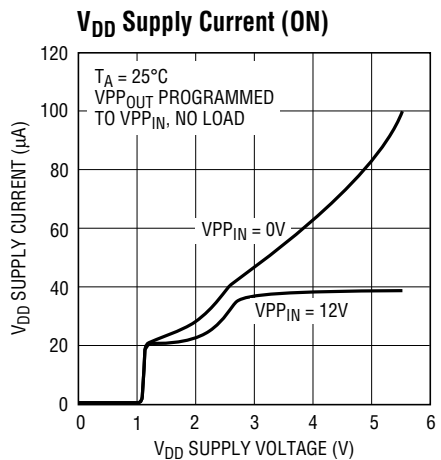
LTC1472 TPC12



LTC1472 TPC13

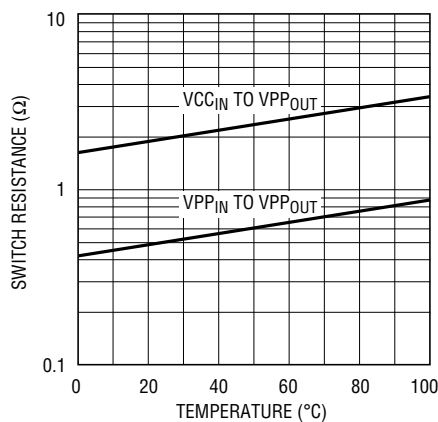


LTC1472 TPC14



LTC1472 TPC15

**Switch Resistances**



LTC1472 TPC16

## PIN FUNCTIONS

### Enable Input (Pins 3,4,7,8)

The two  $V_{CC}$  and two VPP Enable inputs are designed to interface directly with industry standard PCMCIA controllers. They are high impedance CMOS gates with ESD protection diodes to ground, and should not be forced below ground. Both sets of inputs have about 100mV of built-in hysteresis to ensure clean switching between operating modes.

### Shutdown Output (Pin 6)

The LTC1472 is designed to operate *without* continuous 12V power. The gates of the  $V_{CC}$  NMOS switches are powered by charge pumps from the  $5V_{IN}$  supply, and the gates of the VPP NMOS switches are powered by charge pumps powered from the  $V_{DD}$  supply when 12V is not present at the  $VPP_{IN}$  pin (see Application Information for more details). Therefore, the external 12V regulator can be shut down most of the time, and only turned on when programming the socket VPP pin to 12V.

The shutdown output is active high; i.e. the system 12V regulator is shut down when this output is held high and turned on when this output is held low.

### VPP<sub>IN</sub> Supply (Pin 5)

The  $VPP_{IN}$  supply pin serves two purposes. The first purpose is to provide power and gate drive for the  $VPP_{IN}$ - $VPP_{OUT}$  switch. The second purpose is to provide optional 12V gate drive for the  $V_{CC(IN)}$ - $VPP_{OUT}$  switch. If, however, this 12V power is not available, gate drive is obtained automatically from the 5V  $V_{DD}$  supply by an internal 5V to 12V charge pump converter.

### V<sub>DD</sub> Supply (Pin 9)

The  $V_{DD}$  pin provides power for the input, charge pump and control circuitry for the VPP section of the LTC1472 and therefore must be continuously powered. The standby quiescent current is typically 0.1 $\mu$ A when the  $VPP_{OUT}$  pin is programmed to 0V or Hi-Z and only rises to micropower levels when the VPP switches are active.

### V<sub>CC(IN)</sub> Supply (Pin 12)

The  $V_{CC(IN)}$  supply pin is typically connected directly to the  $V_{CC(OUT)}$  pin from the  $V_{CC}$  switch section of the LTC1472. It can also be connected directly to a 3.3V or 5V power supply if desired. This supply pin does not provide any power to the internal control circuitry and is simply the input to the  $V_{CC(IN)}$ - $VPP_{OUT}$  switch and therefore does not consume any power when unloaded or turned off.

### 5V<sub>IN</sub> Supply (Pin 2)

The  $5V_{IN}$  supply pin serves two purposes. The first purpose is as the power supply input for the 5V NMOS switch. The second purpose is to provide power for the input, gate drive and protection circuitry for both the 3.3V and 5V  $V_{CC}$  switches, *this pin must be continuously powered*.

The enable inputs should be turned off (both asserted high or both asserted low) at least 100 $\mu$ s before the  $5V_{IN}$  power is removed to ensure that both  $V_{CC}$  NMOS switch gates are fully discharged and both switches are in the high impedance mode.

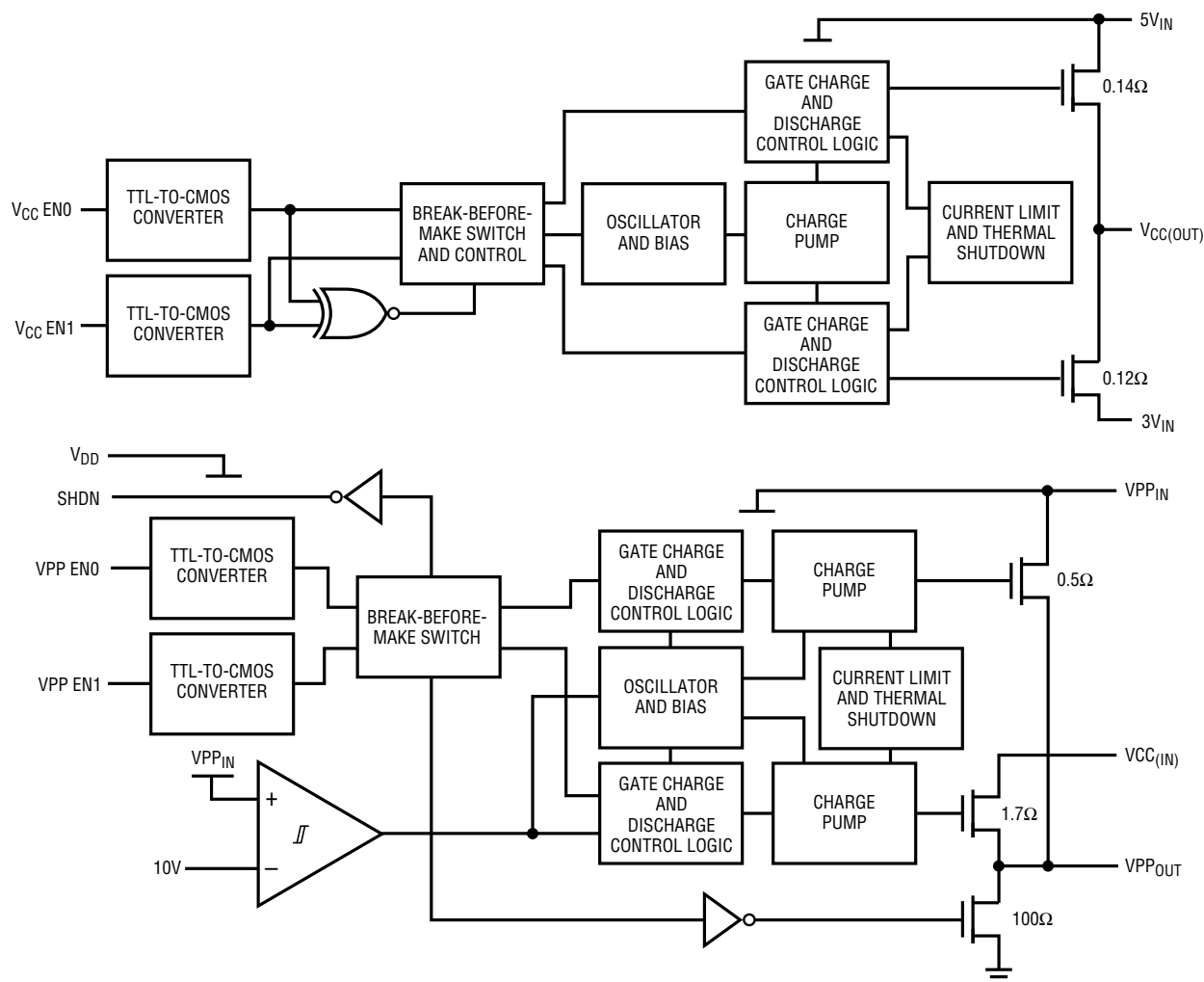
### 3V<sub>IN</sub> Supply (Pins 14,15)

The  $3V_{IN}$  supply pin serves as the power supply input for the 3.3V switch. This pin does not provide any power to the internal control circuitry and therefore does not consume any power when unloaded or turned off.

### V<sub>CC(OUT)</sub> and VPP<sub>OUT</sub> Output (Pins 1,11,16)

The  $V_{CC}$  output of the LTC1472 is switched between the three operating states: OFF, 3.3V, and 5V. The VPP output is switched between four operating states: 0,  $V_{CC}$ , 12V and Hi-Z. Both pins are protected against accidental short-circuit conditions to ground by independent SafeSlot foldback current-limit circuitry which protects the socket, card and the system power supplies against damage. A second level of protection is provided by independent thermal shut down circuitry which protects each switch against overtemperature conditions.

## BLOCK DIAGRAM



## OPERATION

The LTC1472 protected switch matrix is designed to be a complete single slot solution for  $V_{CC}$  and  $V_{PP}$  switching in a PCMCIA compatible card system. The LTC1472 consists of two independent functional sections: the  $V_{CC}$  switching section, and the  $V_{PP}$  switching section.

### THE $V_{CC}$ SWITCHING SECTION

The  $V_{CC}$  switching section of the LTC1472 consist of the following functional blocks:

### $V_{CC}$ Switch Input TTL-CMOS Converters

The LTC1472  $V_{CC}$  inputs are designed to accommodate a wide range of 3V and 5V logic families. The input threshold voltage is approximately 1.4V with approximately 100mV of hysteresis. The inputs enable the bias generator, the gate charge pumps and the protection circuitry which are powered from the  $5V_{IN}$  supply. Therefore, when the inputs are turned off, the entire circuit is powered down and the  $5V_{IN}$  supply current drops below  $1\mu A$ .

## OPERATION

### V<sub>CC</sub> XOR Input Circuitry

The LTC1472 ensures that the 3.3V and 5V switches are never turned on at the same time by employing an XOR function which locks out the 3.3V switch when the 5V switch is turned on, and locks out the 5V switch when the 3.3V switch is turned on. This XOR function also makes it possible for the LTC1472 to work with either active-low or active-high PCMCIA V<sub>CC</sub> switch control logic (see Applications Information for further details).

### V<sub>CC</sub> Break-Before-Make Switch Control

The LTC1472 has built-in delays to ensure that the 3.3V and 5V switch are non-overlapping. Further, the gate charge pumps include circuitry which ramps the NMOS switches on slowly (400 $\mu$ s typical rise time) but turn off much more quickly (typically 10 $\mu$ s).

### V<sub>CC</sub> Bias, Oscillator and Gate Charge Pump

When either the 3.3V or 5V switch is enabled, a bias current generator and high frequency oscillator are turned on. An on-chip capacitive charge pump generates approximately 12V of gate drive for the internal low R<sub>DS(ON)</sub> NMOS V<sub>CC</sub> switches from the 5V<sub>IN</sub> power supply. Therefore, an external 12V supply is not required to switch the V<sub>CC</sub> output. The 5V<sub>IN</sub> supply current drops below 1 $\mu$ A when both switches are turned off.

### V<sub>CC</sub> Gate Charge and Discharge Control

Both V<sub>CC</sub> switches are designed to ramp on slowly (400 $\mu$ s typical rise time). Turn off time is much quicker (typically 10 $\mu$ s).

To ensure that both V<sub>CC</sub> NMOS switch gates are fully discharged, program the switch to the high impedance mode at least 100 $\mu$ s before turning off the 5V<sub>IN</sub> power supply.

### V<sub>CC</sub> Switch Protection

Two levels of protection are designed into each of the power switches in the LTC1472. Both V<sub>CC</sub> switches are protected against accidental short circuits with SafeSlot fold-back current limit circuits which limit the output current to typically 1A when the V<sub>CC(OUT)</sub> output is shorted

to ground. Both switches also have independent thermal shutdown which limits the power dissipation to safe levels.

V<sub>CC</sub> Switch Truth Table

V <sub>CC</sub> EN0	V <sub>CC</sub> EN1	V <sub>CC(OUT)</sub>
0	0	OFF
1	0	5V
0	1	3.3V
1	1	OFF

## THE VPP SWITCHING SECTION

The VPP switching section of the LTC1472 consists of the following functional blocks:

### VPP Switch Input TTL-CMOS Converters

The VPP inputs are designed to accommodate a wide range of 3V and 5V logic families. The input threshold voltage is 1.4V with  $\approx$  100mV of hysteresis. The inputs enable the bias generator, the gate charge pumps and the protection circuitry. When the inputs are turned off, the entire circuit is powered down and the V<sub>DD</sub> and VPP<sub>IN</sub> supply currents drop below 1 $\mu$ A.

### VPP Break-Before-Make Switch Control

The VPP input section has built-in delays to ensure that the VPP switches are non-overlapping. Further, the gate charge pumps include circuitry which ramps the NMOS switches on slowly but turns them off quickly.

### VPP Bias, Oscillator and Gate Charge Pump

When either the VPP<sub>IN</sub>-VPP<sub>OUT</sub> or V<sub>CC(IN)</sub>-VPP<sub>OUT</sub> switch is enabled, a bias current generator and high frequency oscillator are turned on. An on-chip capacitive charge pump generates approximately 23V of gate drive for the internal low R<sub>DS(ON)</sub> NMOS VPP<sub>IN</sub>-VPP<sub>OUT</sub> switch from the VPP<sub>IN</sub> power supply. The gate of the V<sub>CC(IN)</sub>-VPP<sub>OUT</sub> NMOS switch is either powered by the external 12V regulator (if left on) or automatically from a built-in charge pump powered from the V<sub>DD</sub> supply when the external 12V supply drops below 10V. The V<sub>DD</sub> supply current drops below 1 $\mu$ A when switched to either the 0V or Hi-Z mode.





## APPLICATIONS INFORMATION

### Output Capacitors

The  $V_{CC(OUT)}$  pin is designed to ramp on slowly, typically 400 $\mu$ s rise time. Therefore, capacitors as large as 150 $\mu$ F can be driven without producing voltage spikes on the  $5V_{IN}$  or  $3V_{IN}$  supply pins (see graphs in Typical Performance Characteristics). The  $V_{CC(OUT)}$  pin should have a 0.1 $\mu$ F to 1 $\mu$ F capacitor for noise reduction and smoothing.

The  $VPP_{OUT}$  pin should have a 0.01 $\mu$ F to 0.1 $\mu$ F capacitor for noise reduction. The  $VPP_{IN}$  capacitors should be at least equal to the  $VPP_{OUT}$  capacitors to ensure smooth transitions between output voltages without creating spikes on the system power supply lines.

### Supply Sequencing

Because the 5V supply is the source of power for both the  $V_{CC}$  and  $VPP$  switch control logic, it is best to sequence the power supplies such that the 5V supply is powered before or simultaneous to the application of 3.3V or 12V power.

It is interesting to note however, that all of the switches in the LTC1472 are NMOS transistors which require charge pumps to generate gate voltages higher than the supply rails for full enhancement. Because the gate voltages start

a 0V when the supplies are first activated, the switches always start in the off state and do not produce glitches at the output when powered.

Some PCMCIA switch matrix products employ PMOS switches for 12V  $VPP$  control and great care must be taken to ensure that the 5V control logic is powered before the 12V supply is turned on. If this sequence is not followed, the PMOS  $VPP$  switch gate may start at ground potential and the  $VPP$  output may be inadvertently forced to 12V.

Although, not advisable, it is possible to power the 12V  $VPP_{IN}$  supply pin of the LTC1472 prior to application of 5V power. Only about 50 $\mu$ A flows to the  $VPP_{OUT}$  pin under these conditions.

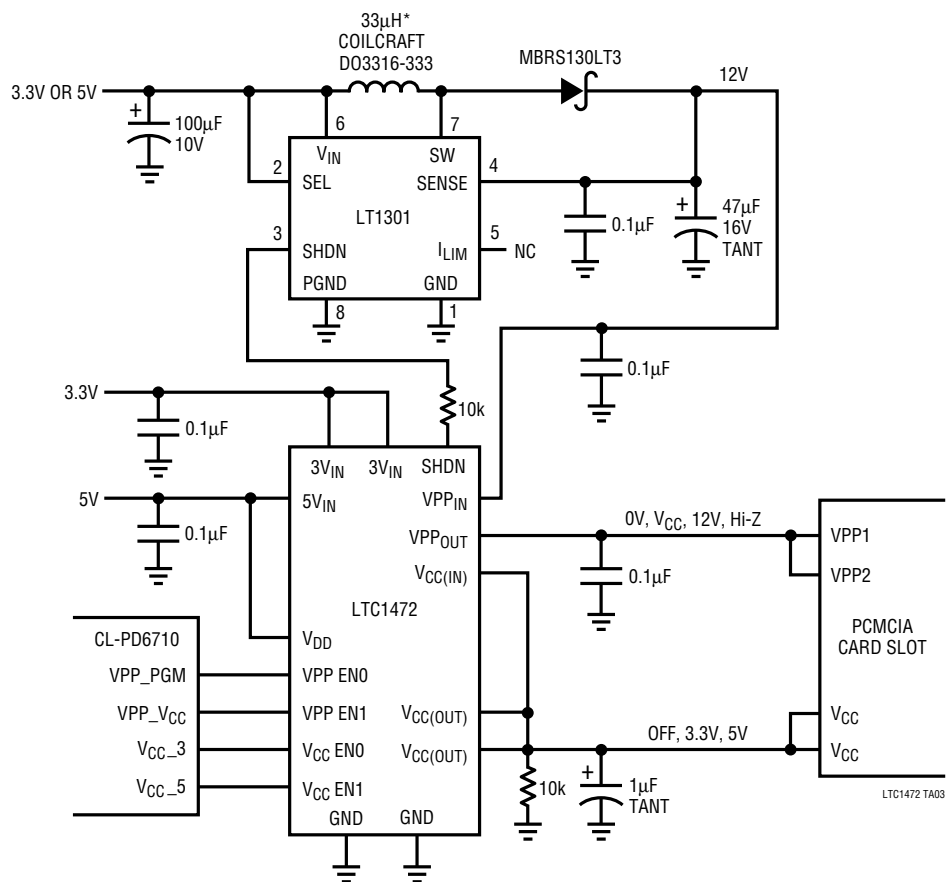
If the 5V supply must be turned off, it is important to program all switches to the Hi-Z or 0V state at least 100 $\mu$ s before the 5V power is removed to ensure that all NMOS switch gates are fully discharged to 0V.

Whenever possible however, it is best to leave the  $5V_{IN}$  and  $V_{DD}$  pins continuously powered. The LTC1472 quiescent current drops to < 1 $\mu$ A with all the switches turned off and therefore no 5V power is consumed in the standby mode.



# TYPICAL APPLICATIONS

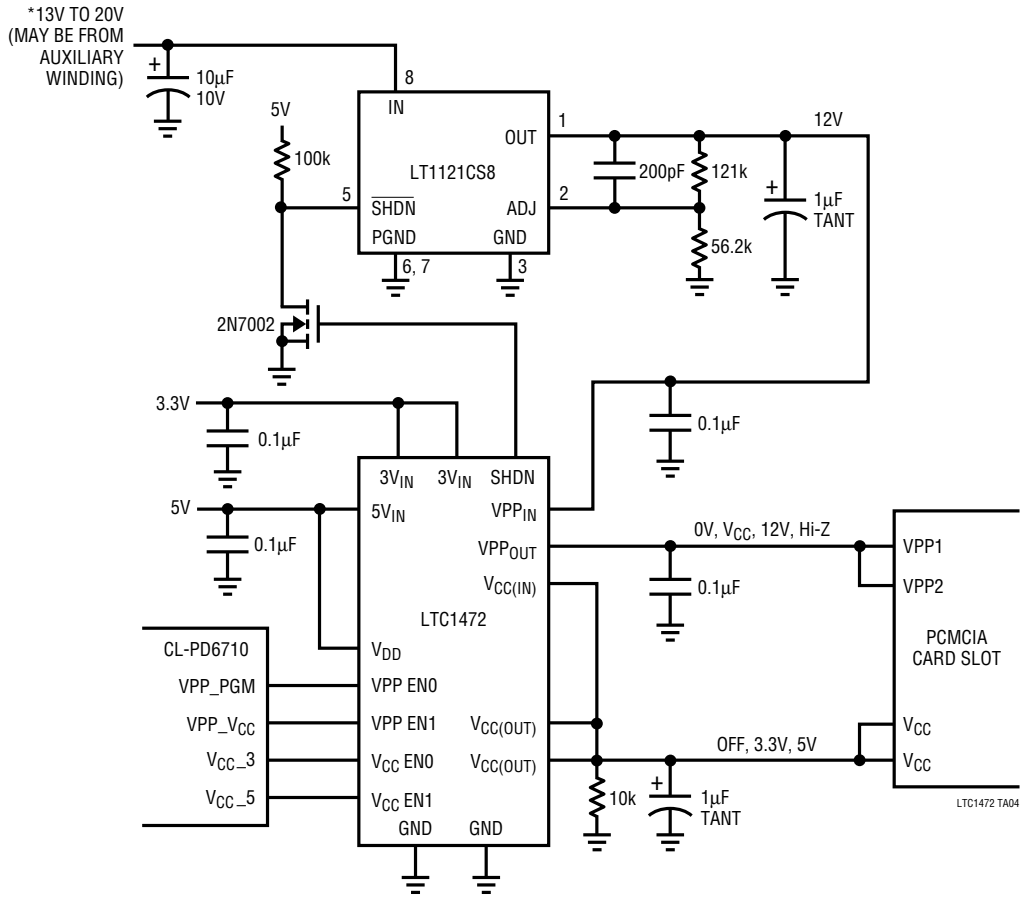
**Single Protected PCMCIA Power Management System  
Using the LT1301 Powered from 3.3V or 5V**



\*FOR 5V TO 12V CONVERSION USE 10µH, COILCRAFT D01608-103. SEE LT1301 DATA SHEET FOR MORE DETAILED INFORMATION ON INDUCTANCE AND CAPACITOR SELECTION.

TYPICAL APPLICATIONS

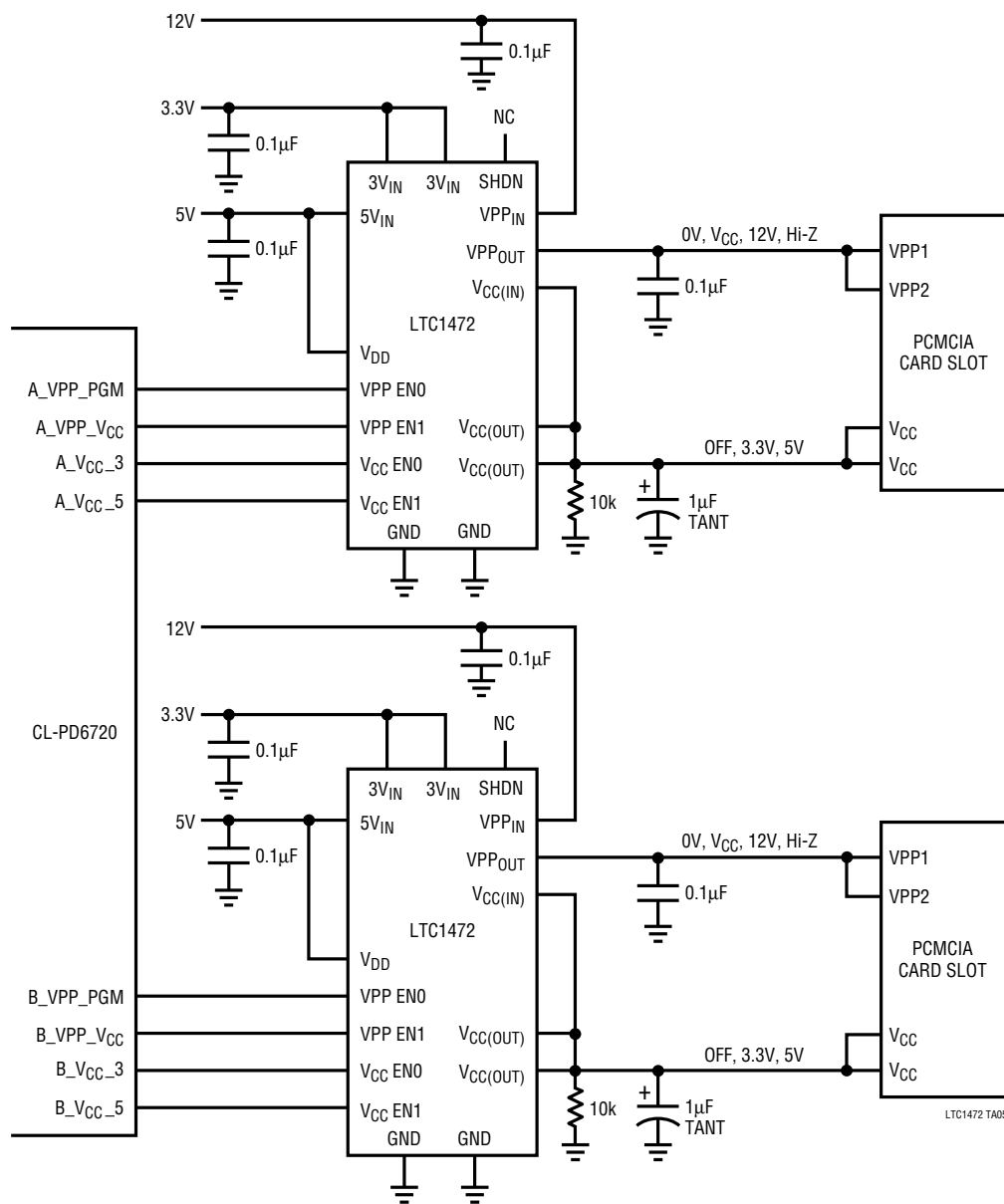
Single Protected PCMCIA Power Management System  
Using the LT1121 Powered from an Auxiliary Winding for 12V VPP Power



\*SEE THE LTC1142 DATA SHEET FOR AN EXAMPLE OF A 3.3V/5V DUAL REGULATOR WITH AUXILIARY WINDING 15V OUTPUT

# TYPICAL APPLICATIONS

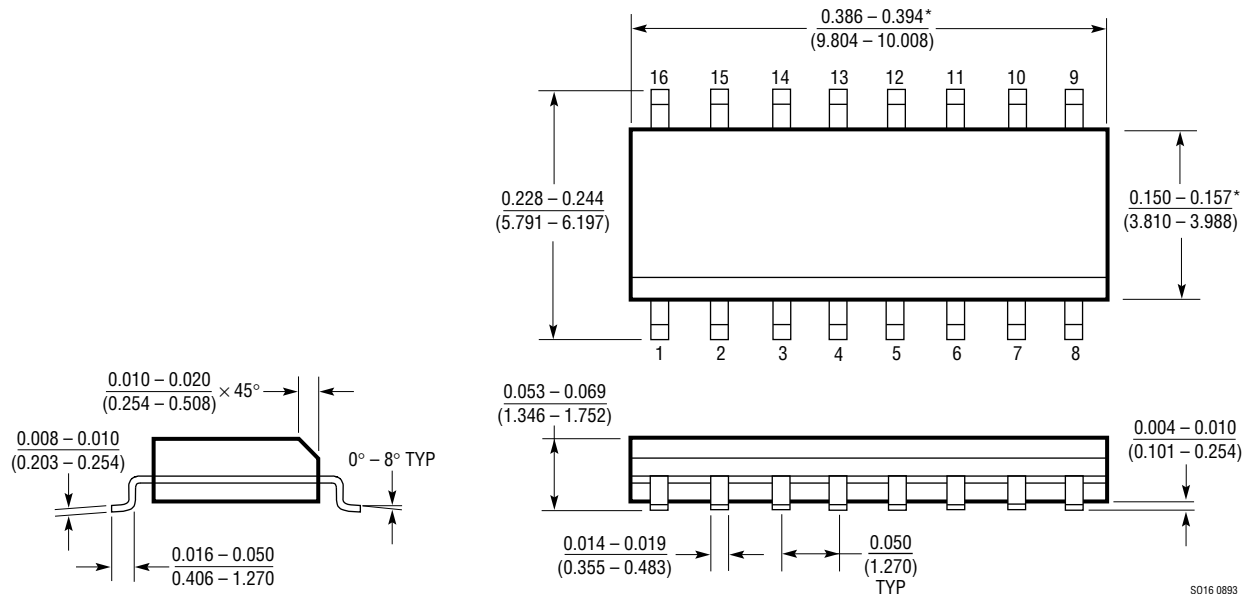
**Dual Protected PCMCIA Power Management System  
Powered by System 12V Supply**



LTC1472 TA05

**PACKAGE DESCRIPTION** Dimensions in inches (millimeters) unless otherwise noted.

**S-Package  
16-lead Plastic SOIC**



\*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.  
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCH (0.15mm).

**RELATED PARTS**

See PCMCIA Product Family table on the first page of this data sheet.