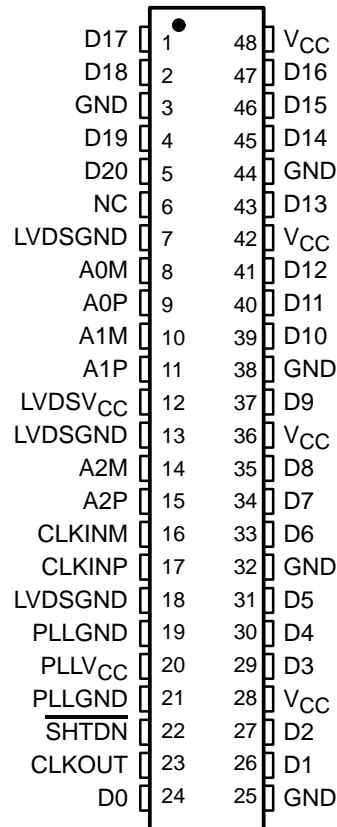


- 3:21 Data Channel Expansion at up to 163 Million Bytes per Second Throughput
- Suited for SVGA, XGA, or SXGA Display Data Transmission From Controller to Display With Very Low EMI
- 3 Data Channels and Clock Low-Voltage Differential Channels In and 21 Data and Clock Low-Voltage TTL Channels Out
- Operates From a Single 3.3-V Supply
- Tolerates 4-kV HBM ESD
- Packaged in Thin Shrink Small-Outline Package (TSSOP) With 20-Mil Terminal Pitch
- Consumes Less Than 1 mW When Disabled
- Wide Phase-Lock Input Frequency Range 31 MHz to 68 MHz
- No External Components Required for PLL
- Inputs Meet or Exceed the Standard Requirements of ANSI EIA/TIA-644 Standard
- Improved Replacement for the DS90C364 and SN75LVDS86
- Improved Jitter Tolerance
- Available in Q-Temp Automotive High Reliability Automotive Applications Configuration Control / Print Support Qualification to Automotive Standards

DGG PACKAGE  
(TOP VIEW)



NC – Not connected

## description

The SN65LVDS86AQ/SN75LVDS86A FlatLink receiver contains three serial-in 7-bit parallel-out shift registers and four low-voltage differential signaling (LVDS) line receivers in a single integrated circuit. These functions allow receipt of synchronous data from a compatible transmitter, such as the SN75LVDS81, '83, '84, or '85, over four balanced-pair conductors and expansion to 21 bits of single-ended low-voltage LVTTTL synchronous data at a lower transfer rate.

When receiving, the high-speed LVDS data is received and loaded into registers at seven times the LVDS input clock (CLKIN) rate. The data is then unloaded to a 21-bit wide LVTTTL parallel bus at the CLKIN rate. The 'LVDS86A presents valid data on the falling edge of the output clock (CLKOUT).

The 'LVDS86A requires only four line-termination resistors for the differential inputs and little or no control. The data bus appears the same at the input to the transmitter and output of the receiver with the data transmission transparent to the user(s). The only user intervention is the possible use of the shutdown/clear (SHTDN) active-low input to inhibit the clock and shut off the LVDS receivers for lower power consumption. A low level on this signal clears all internal registers to a low level.

The SN75LVDS86A is characterized for operation over ambient free-air temperatures of 0°C to 70°C. The SN65LVDS86AQ is characterized for operation over the full Automotive temperature range of –40°C to 125°C.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

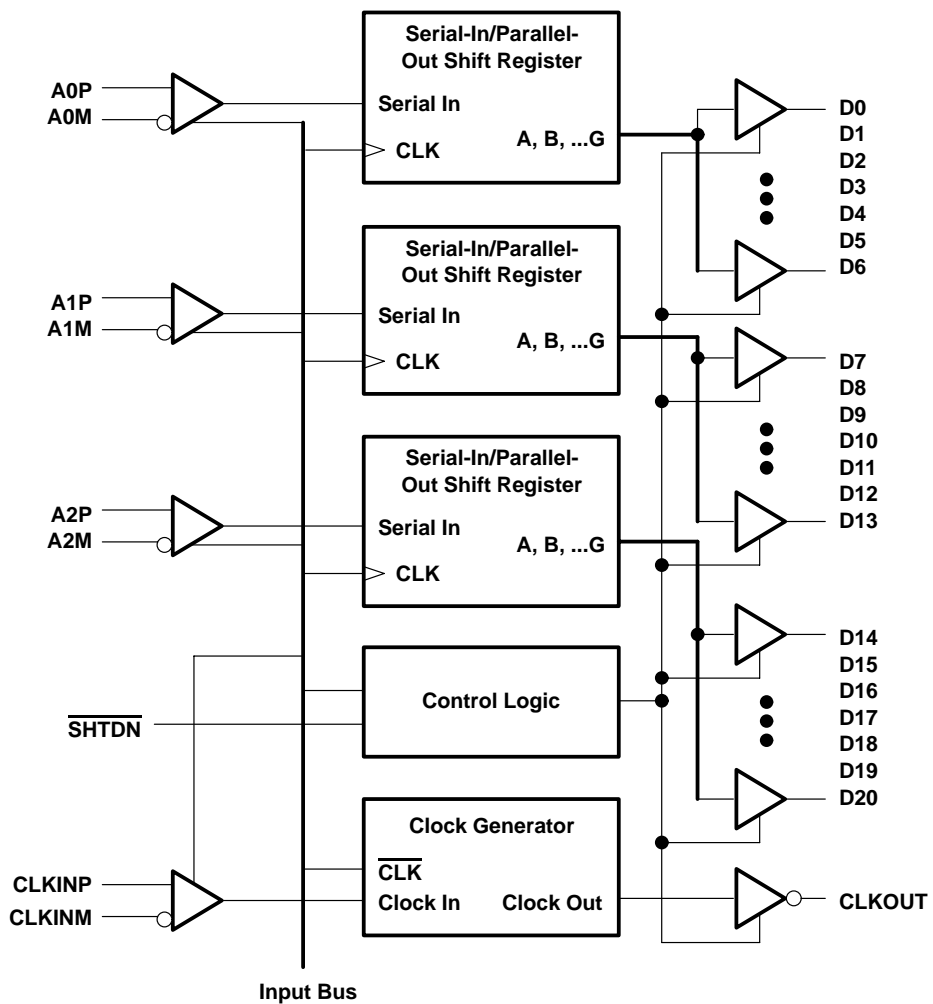
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# SN65LVDS86AQ, SN75LVDS86A FLATLINK™ RECEIVER

SLLS318B – NOVEMBER 1998 – REVISED JANUARY 2001

## functional block diagram



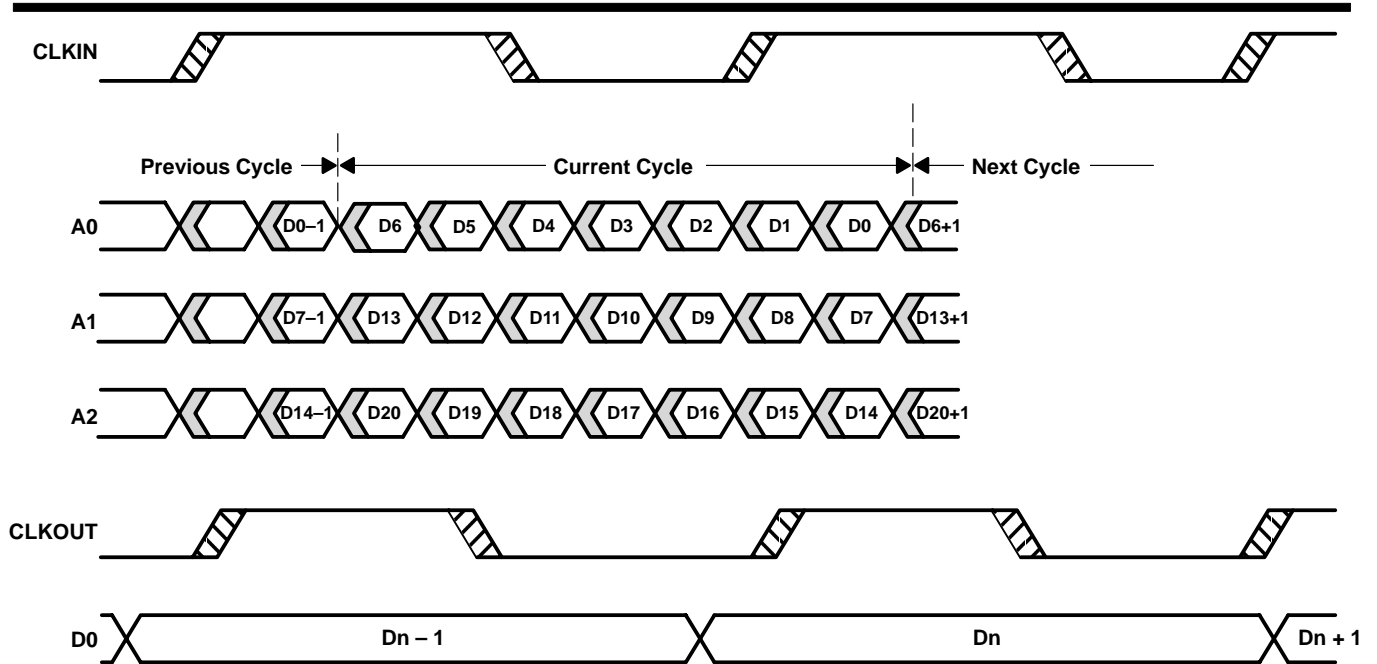
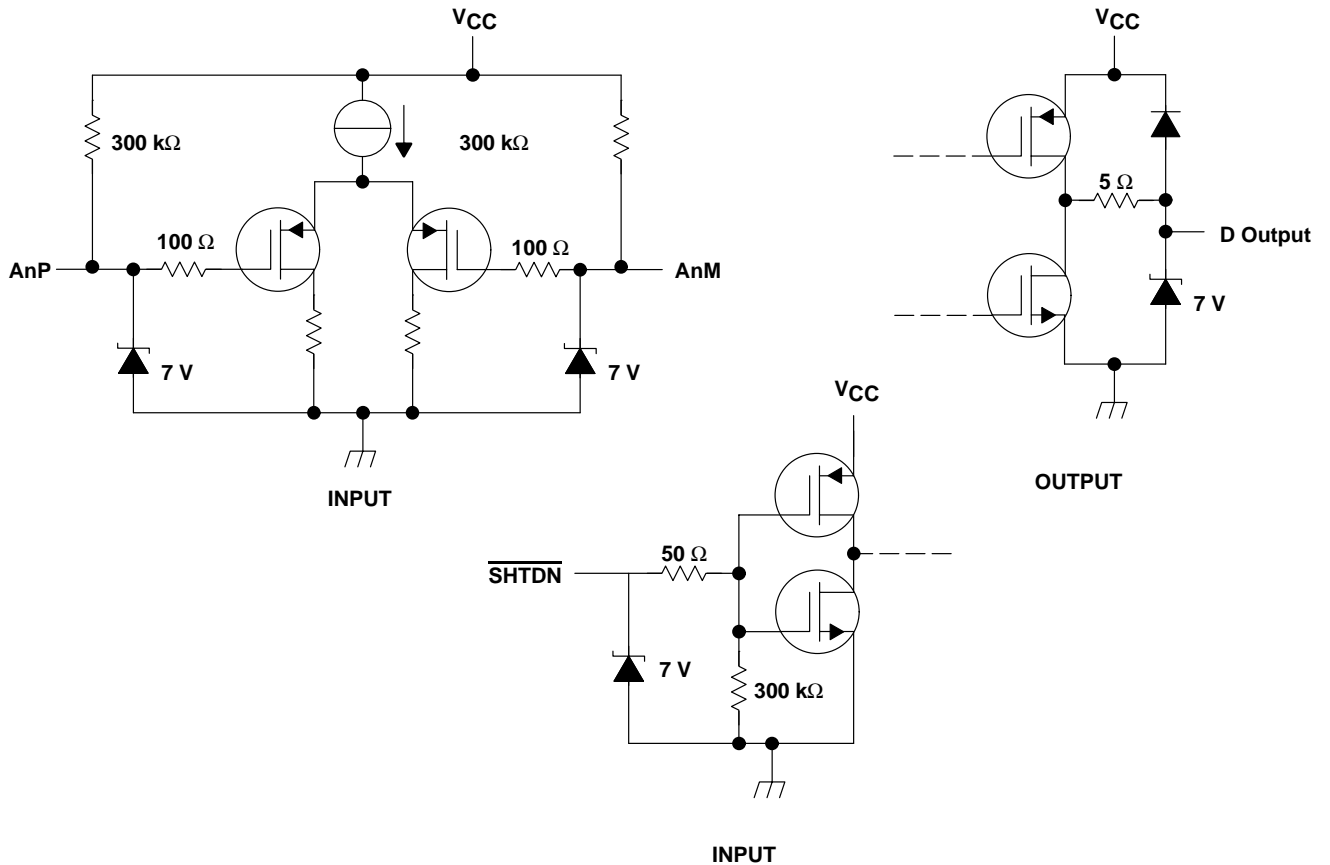


Figure 1. SN65LVDS86AQ/SN75LVDS86A Load and Shift Timing Sequences

equivalent input and output schematic diagrams





**electrical characteristics over recommended operating conditions (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT	
V <sub>IT+</sub>	Positive-going differential input threshold voltage				100	mV	
V <sub>IT-</sub>	Negative-going differential input threshold voltage‡		-100			mV	
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -4 mA	2.4			V	
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 4 mA			0.4	V	
I <sub>CC</sub>	Quiescent current (average)	Disabled, All inputs to GND			280	μA	
		Enabled, AnP = 1 V, AnM = 1.4 V, t <sub>C</sub> = 15.38 ns		33	40	mA	
		Enabled, C <sub>L</sub> = 8 pF, Grayscale pattern (see Figure 3), t <sub>C</sub> = 15.38 ns			43		mA
		Enabled, C <sub>L</sub> = 8 pF, Worst-case pattern (see Figure 4) t <sub>C</sub> = 15.38 ns			68		mA
I <sub>IH</sub>	High-level input current ( $\overline{\text{SHTDN}}$ )	V <sub>IH</sub> = V <sub>CC</sub>			±20	μA	
I <sub>IL</sub>	Low-level input current ( $\overline{\text{SHTDN}}$ )	V <sub>IL</sub> = 0	SN75LVDS86A		±20	μA	
			SN65LVDS86AQ		±25	μA	
I <sub>I</sub>	Input current A inputs	0 ≤ V <sub>I</sub> ≤ 2.4 V			±20	μA	
I <sub>OZ</sub>	High-impedance output current	V <sub>O</sub> = 0 or V <sub>CC</sub>			±10	μA	

† All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for the negative-going input voltage threshold only.

**switching characteristics over recommended operating conditions (unless otherwise noted)**

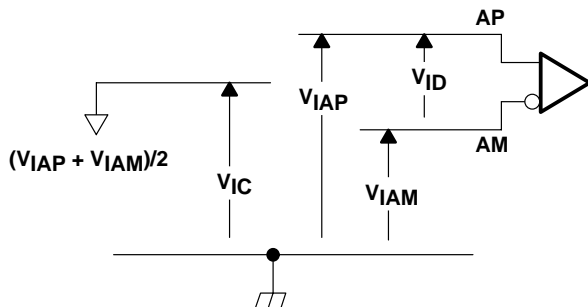
PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t <sub>su</sub>	Setup time, D0 – D20 to CLKOUT↓	C <sub>L</sub> = 8 pF, See Figure 5	5			ns
t <sub>h</sub>	Data hold time, CLKOUT↓ to D0 – D20		5			ns
t <sub>(RSKM)</sub>	Receiver input skew margin§ (see Figure 7)	t <sub>C</sub> = 15.38 ns (±0.2%),  Input clock jitter  < 50 ps¶	550	700		ps
t <sub>d</sub>	Delay time, CLKIN↑ to CLKOUT↓ (see Figure 7)	V <sub>CC</sub> = 3.3 V, t <sub>C</sub> = 15.38 ns (±0.2%), T <sub>A</sub> = 25°C	3	5	7	ns
t <sub>en</sub>	Enable time, $\overline{\text{SHTDN}}$ to phase lock	See Figure 7		1		ms
t <sub>dis</sub>	Disable time, $\overline{\text{SHTDN}}$ to off state	See Figure 8		400		ns
t <sub>t</sub>	Transition time, output (10% to 90% t <sub>r</sub> or t <sub>f</sub> ) (data only)	C <sub>L</sub> = 8 pF		3		ns
t <sub>t</sub>	Transition time, output (10% to 90% t <sub>r</sub> or t <sub>f</sub> ) (clock only)	C <sub>L</sub> = 8 pF		1.5		ns
t <sub>w</sub>	Pulse duration, output clock			0.50 t <sub>C</sub>		ns

† All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

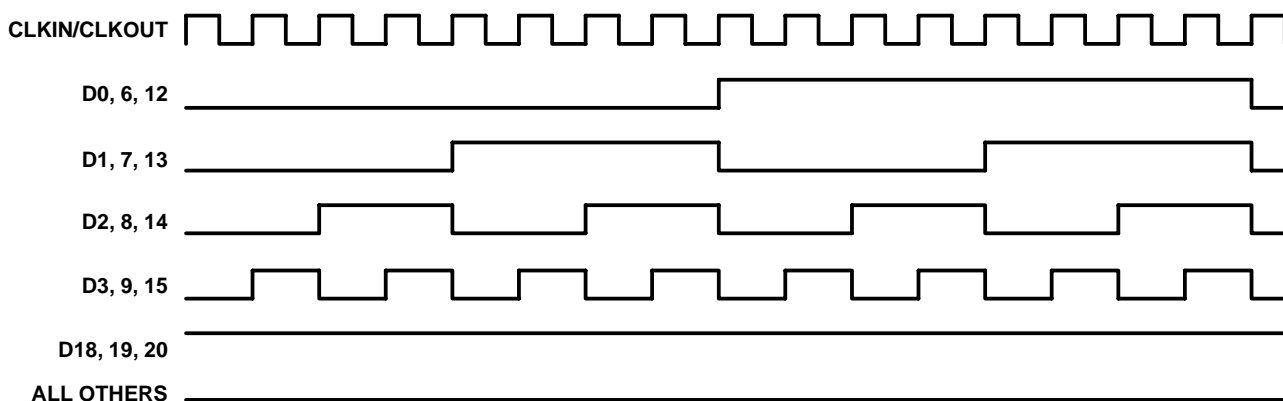
§ The parameter t<sub>(RSKM)</sub> is the timing margin available to allocate to the transmitter and interconnection skews and clock jitter. The value of this parameter at clock periods other than 15.38 ns can be calculated from t<sub>(RSKM)</sub> = t<sub>C</sub>/14 – 550 ps.

¶ |Input clock jitter| is the magnitude of the change in input clock period.

**PARAMETER MEASUREMENT INFORMATION**

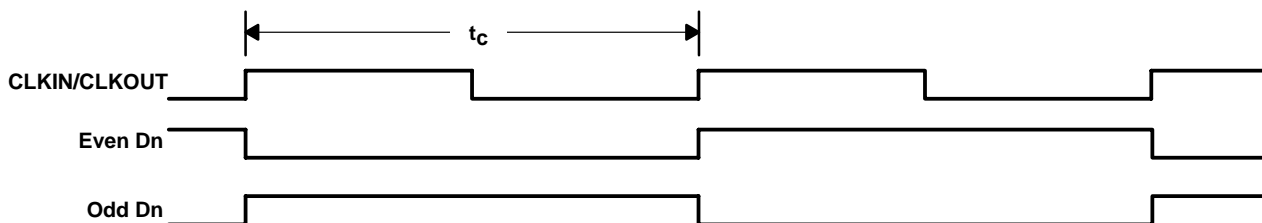


**Figure 2. Voltage Definitions**



NOTE A: The 16-grayscale test-pattern test device power consumption for a typical display pattern.

**Figure 3. 16-Grayscale Test-Pattern Waveforms**



NOTE A: The worst-case test pattern produces nearly the maximum switching frequency for all of the LVTTTL outputs.

**Figure 4. Worst-Case Test-Pattern Waveforms**

PARAMETER MEASUREMENT INFORMATION

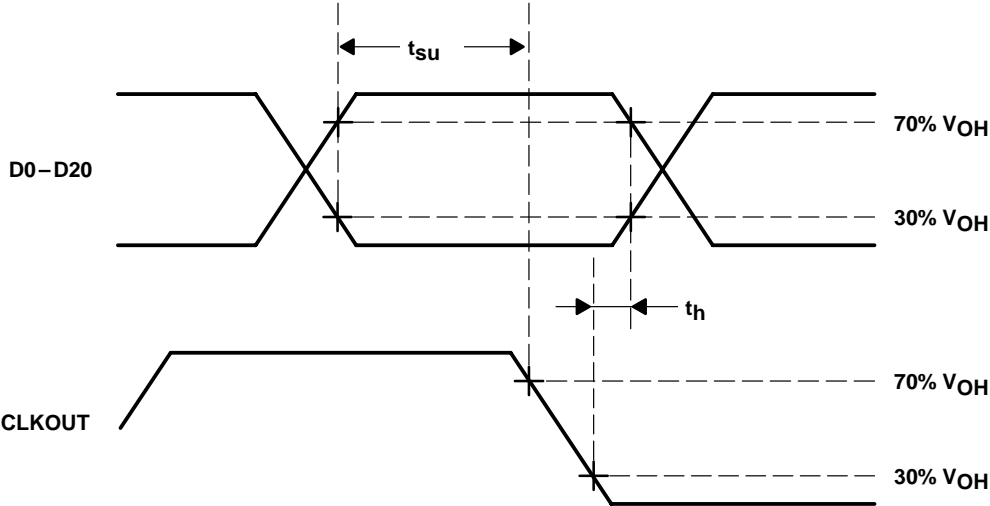
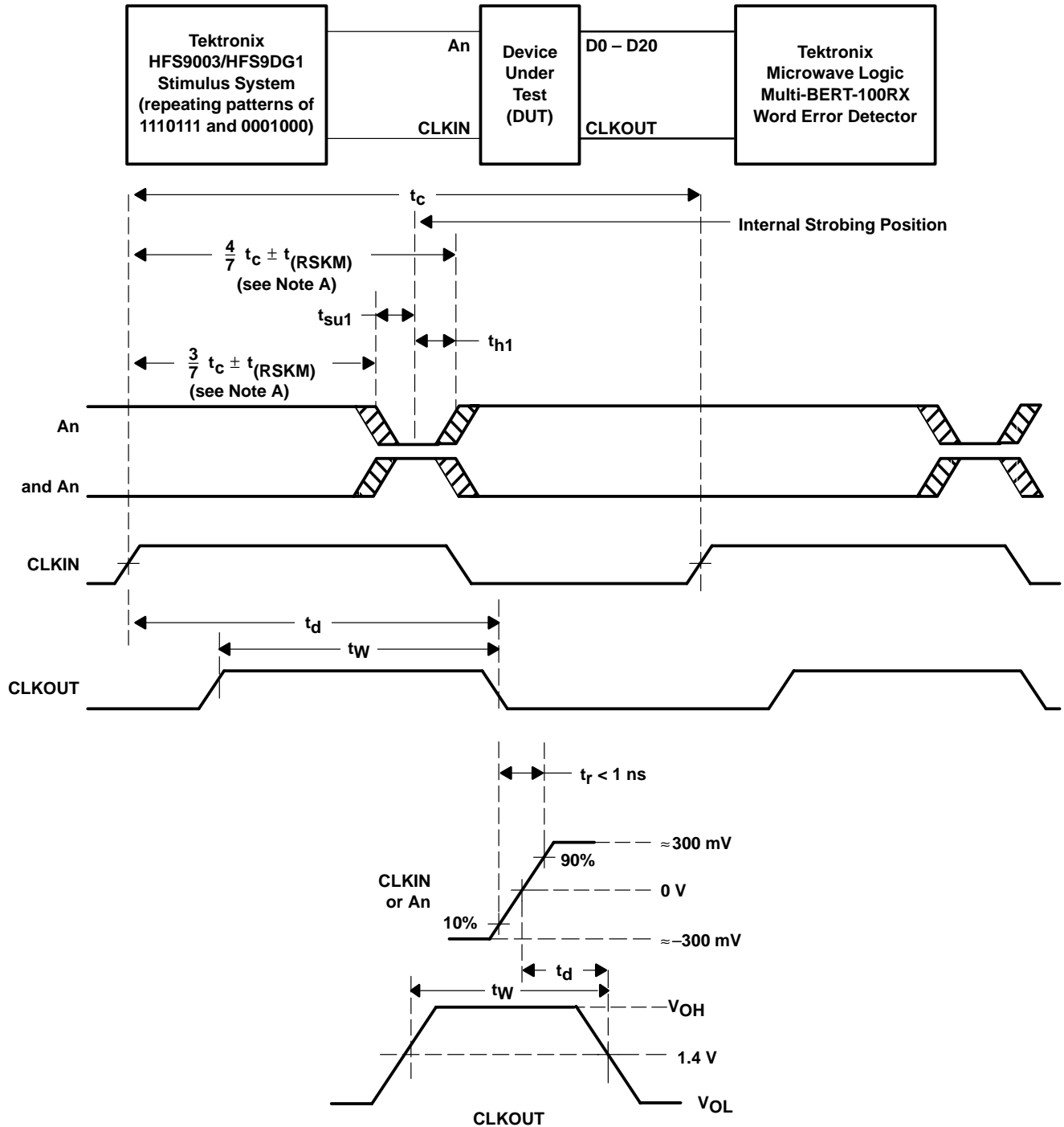


Figure 5. Setup and Hold Time Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE A: CLKIN is advanced or delayed with respect to data until errors are observed at the receiver outputs. The advance or delay is then reduced until there are no data errors observed. The magnitude of the advance or delay is  $t_{(RSKM)}$ .

Figure 6. Receiver Input Skew Margin, Setup/Hold Time, and Delay Time Definitions

PARAMETER MEASUREMENT INFORMATION

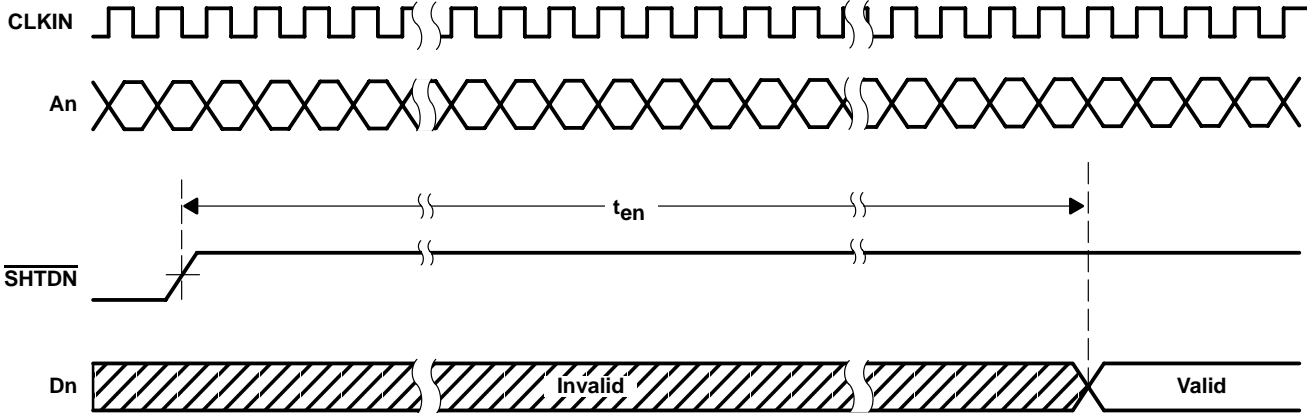


Figure 7. Enable Time Waveforms

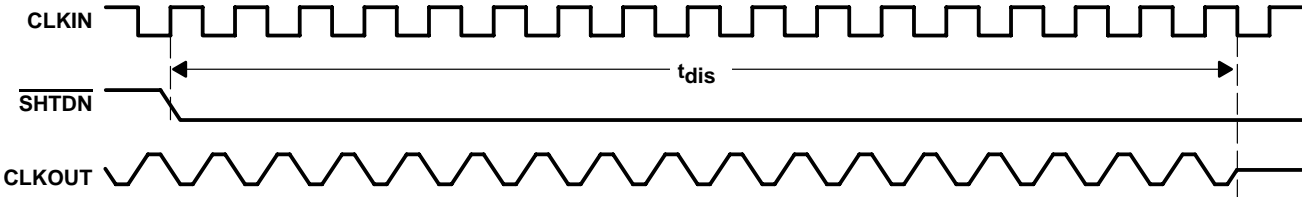


Figure 8. Disable Time Waveforms

TYPICAL CHARACTERISTICS

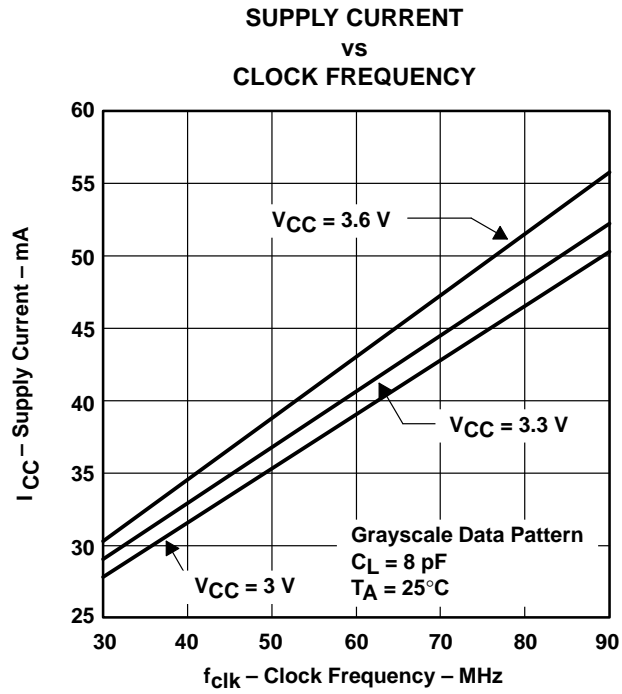
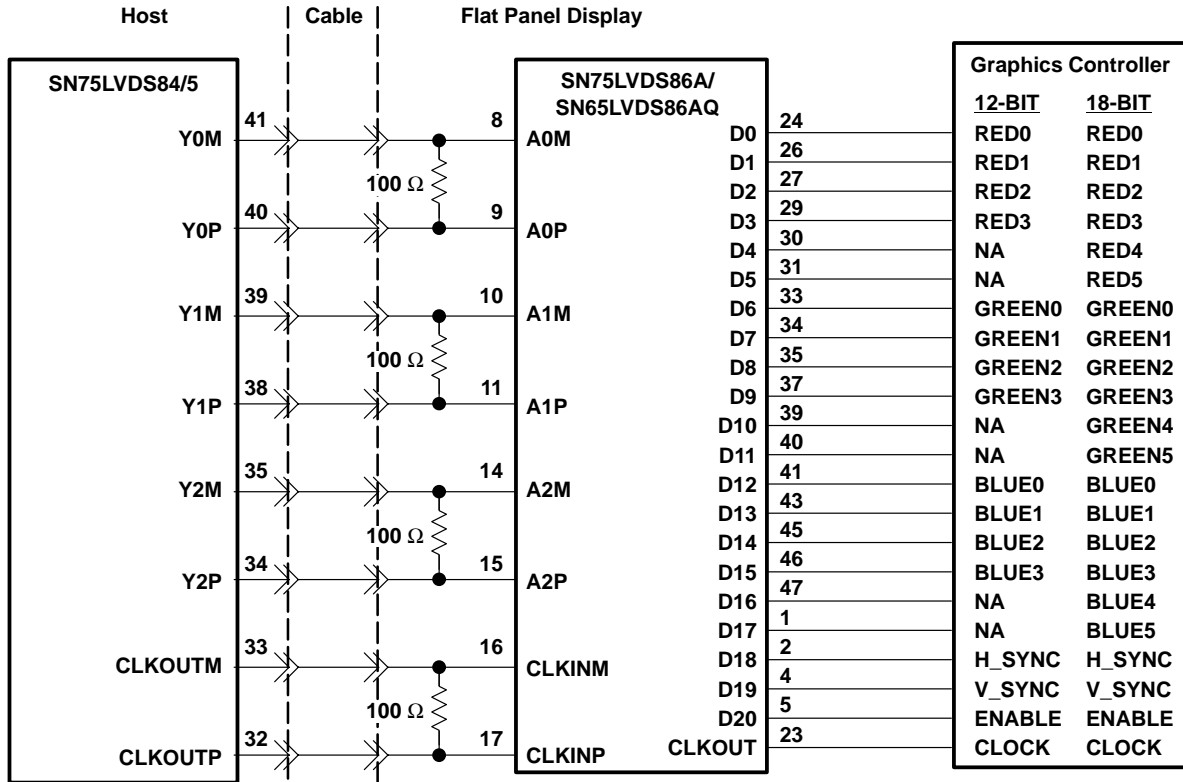


Figure 9. RMS Grayscale  $I_{CC}$  vs Clock Frequency

**APPLICATION INFORMATION**



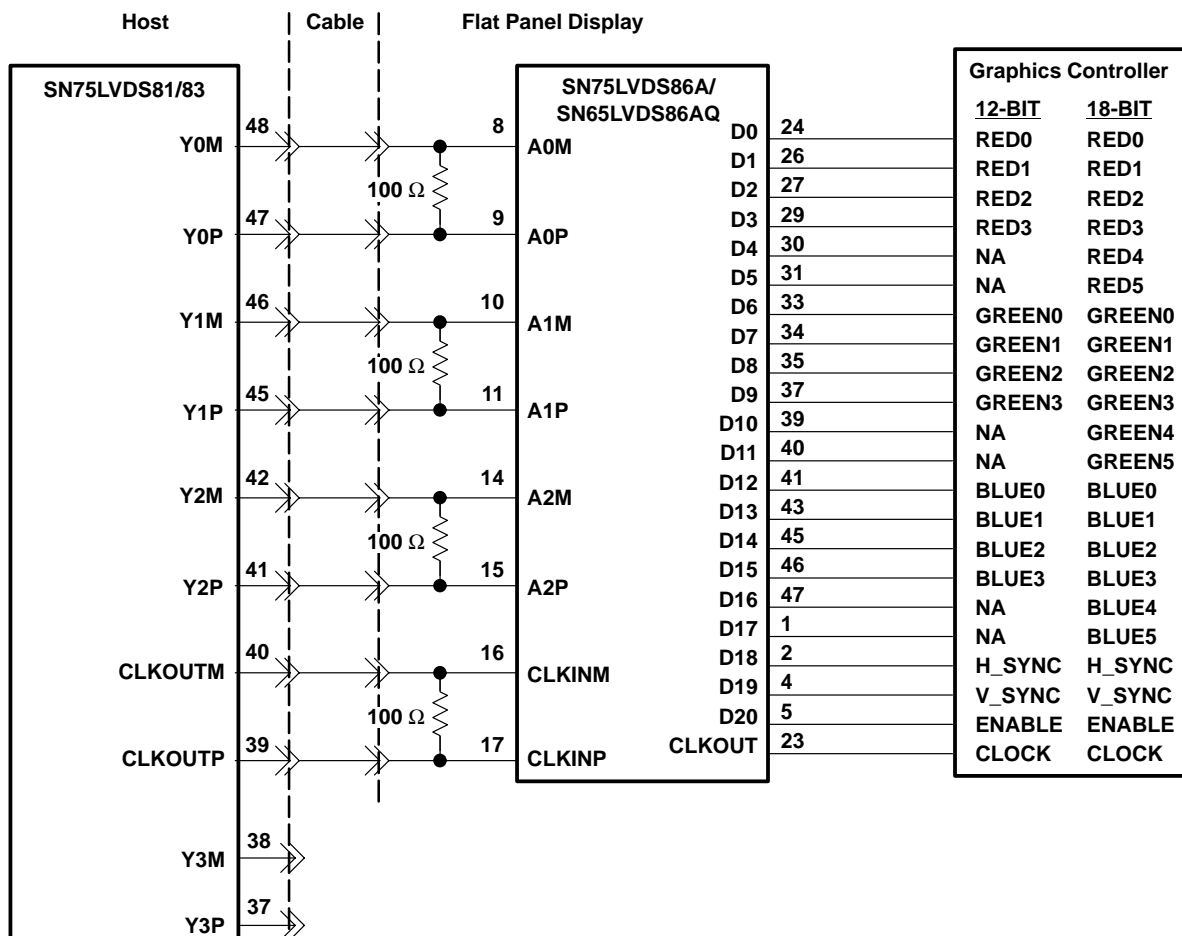
NOTES: A. The four 100-Ω terminating resistors are recommended to be 0603 types.  
 B. NA – not applicable, these unused inputs should be left open.

**Figure 10. 18-Bit Color Host to Flat Panel Display Application**

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## APPLICATION INFORMATION



- NOTES: A. The four 100-Ω terminating resistors are recommended to be 0603 types.  
B. NA – not applicable, these unused inputs should be left open.

**Figure 11. 24-Bit Color Host to 18-Bit Color LCD Panel Display Application**

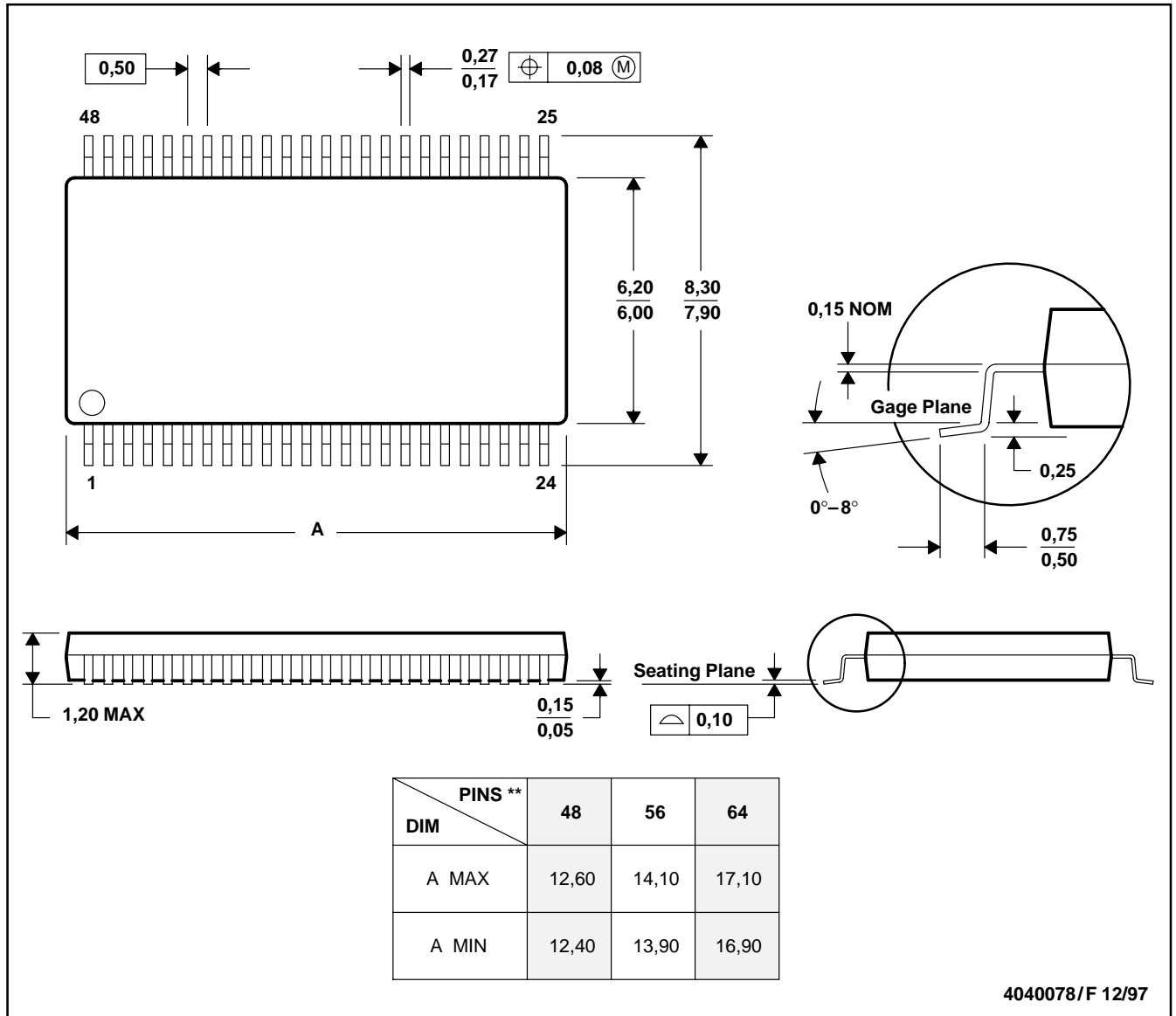
See the *FAtLink Designer's Guide* (SLLA012) for more application information.

MECHANICAL INFORMATION

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PIN SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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