

SN74ALVCH162820

3.3-V 10-BIT FLIP-FLOP WITH DUAL OUTPUTS AND 3-STATE OUTPUTS

SCES012G – JULY 1995 – REVISED NOVEMBER 1999

- Member of the Texas Instruments *Widebus™* Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Output Ports Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

NOTE: For tape and reel order entry:
The DGGR package is abbreviated to GR.

description

This 10-bit flip-flop is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH162820 flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs.

A buffered output-enable (\overline{OE}) input can be used to place the ten outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

\overline{OE} does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The outputs, which are designed to sink up to 12 mA, include equivalent 26-Ω resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

DGG OR DL PACKAGE
(TOP VIEW)

$\overline{1OE}$	1	56	CLK
1Q1	2	55	D1
1Q2	3	54	NC
GND	4	53	GND
2Q1	5	52	D2
2Q2	6	51	NC
V_{CC}	7	50	V_{CC}
3Q1	8	49	D3
3Q2	9	48	NC
4Q1	10	47	D4
GND	11	46	GND
4Q2	12	45	NC
5Q1	13	44	D5
5Q2	14	43	NC
6Q1	15	42	D6
6Q2	16	41	NC
7Q1	17	40	D7
GND	18	39	GND
7Q2	19	38	NC
8Q1	20	37	D8
8Q2	21	36	NC
V_{CC}	22	35	V_{CC}
9Q1	23	34	D9
9Q2	24	33	NC
GND	25	32	GND
10Q1	26	31	D10
10Q2	27	30	NC
$\overline{2OE}$	28	29	NC

NC – No internal connection



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description (continued)

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

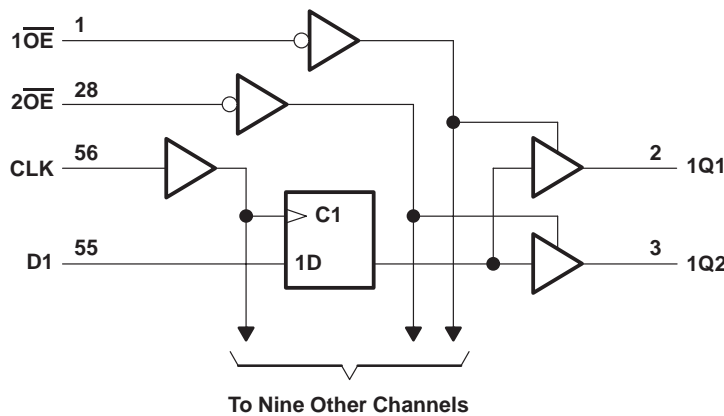
The SN74ALVCH162820 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{\text{OE}}_n^{\dagger}$	CLK	D	Q
L	\uparrow	H	H
L	\uparrow	L	L
L	L	X	Q_0
H	X	X	Z

$\dagger n = 1, 2$

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	$-0.5\text{ V to }4.6\text{ V}$
Input voltage range, V_I (see Note 1)	$-0.5\text{ V to }4.6\text{ V}$
Output voltage range, V_O (see Notes 1 and 2)	$-0.5\text{ V to }V_{CC} + 0.5\text{ V}$
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Continuous output current, I_O	$\pm 50\text{ mA}$
Continuous current through each V_{CC} or GND	$\pm 100\text{ mA}$
Package thermal impedance, θ_{JA} (see Note 3): DGG package	64°C/W
DL package	56°C/W
Storage temperature range, T_{stg}	$-65^{\circ}\text{C to }150^{\circ}\text{C}$

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 4.6 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51.

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recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	1.65	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	1.7	
		V _{CC} = 2.7 V to 3.6 V	2	
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	0.7	
		V _{CC} = 2.7 V to 3.6 V	0.8	
V _I	Input voltage	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65 V	-2	mA
		V _{CC} = 2.3 V	-6	
		V _{CC} = 2.7 V	-8	
		V _{CC} = 3 V	-12	
I _{OL}	Low-level output current	V _{CC} = 1.65 V	2	mA
		V _{CC} = 2.3 V	6	
		V _{CC} = 2.7 V	8	
		V _{CC} = 3 V	12	
Δt/Δv	Input transition rise or fall rate		10	ns/V
T _A	Operating free-air temperature	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP†	MAX	UNIT
V _{OH}	I _{OH} = -100 µA	1.65 V to 3.6 V	V _{CC} -0.2			V
	I _{OH} = -2 mA	1.65 V	1.2			
	I _{OH} = -4 mA	2.3 V	1.9			
	I _{OH} = -6 mA	2.3 V	1.7			
		3 V	2.4			
	I _{OH} = -8 mA	2.7 V	2			
I _{OH} = -12 mA	3 V	2				
V _{OL}	I _{OL} = 100 µA	1.65 V to 3.6 V			0.2	V
	I _{OL} = 2 mA	1.65 V			0.45	
	I _{OL} = 4 mA	2.3 V			0.4	
	I _{OL} = 6 mA	2.3 V			0.55	
		3 V			0.55	
	I _{OL} = 8 mA	2.7 V			0.6	
I _{OL} = 12 mA	3 V			0.8		
I _I	V _I = V _{CC} or GND	3.6 V			±5	µA
I _I (hold)	V _I = 0.58 V	1.65 V	25			µA
	V _I = 1.07 V	1.65 V	-25			
	V _I = 0.7 V	2.3 V	45			
	V _I = 1.7 V	2.3 V	-45			
	V _I = 0.8 V	3 V	75			
	V _I = 2 V	3 V	-75			
	V _I = 0 to 3.6 V‡	3.6 V			±500	
I _{OZ}	V _O = V _{CC} or GND	3.6 V			±10	µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			40	µA
ΔI _{CC}	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V			750	µA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V		3.5	pF
	Data inputs				6	
C _O	Outputs	V _O = V _{CC} or GND	3.3 V		7	pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

		V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	§		150		150		150		MHz
t _w	Pulse duration, CLK high or low	§		3.3		3.3		3.3		ns
t _{su}	Setup time, data before CLK↑	§		1.7		1.8		1.4		ns
t _h	Hold time, data after CLK↑	§		1.1		1.1		1		ns

§ This information was not available at the time of publication.



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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		150		150		150		MHz
t _{pd}	CLK	Q		†	1	6.4		6.2	1	5.4	ns
t _{en}	$\overline{\text{OE}}$	Q		†	1	6.9		6.8	1	5.6	ns
t _{dis}	$\overline{\text{OE}}$	Q		†	1	6.2		5.5	1	5	ns

† This information was not available at the time of publication.

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT
			TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance per flip-flop	All outputs enabled	†	68	66	pF
		All outputs disabled	†	39	47	

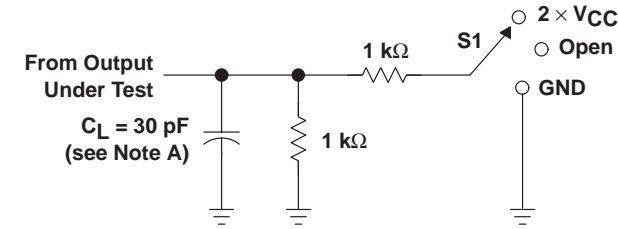
† This information was not available at the time of publication.



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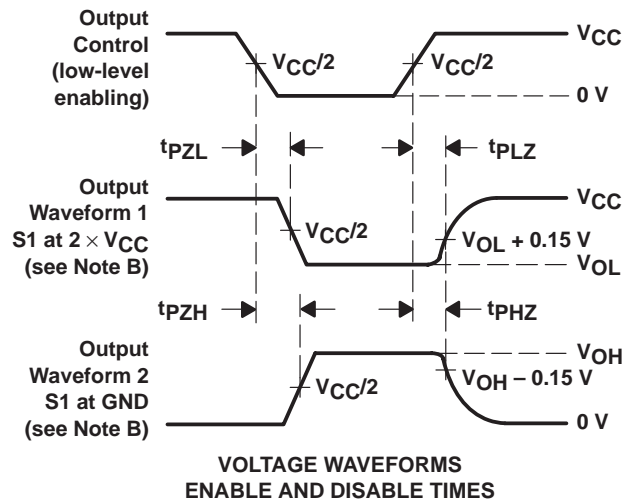
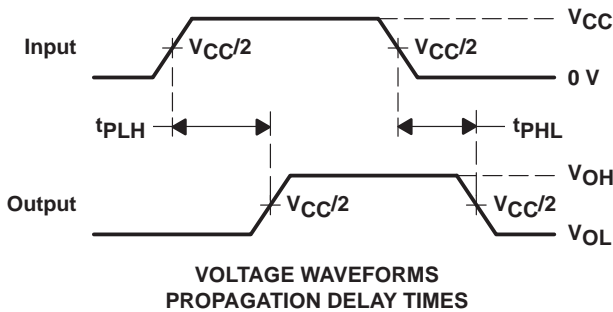
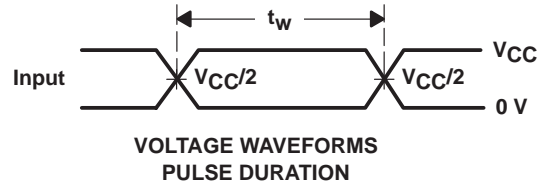
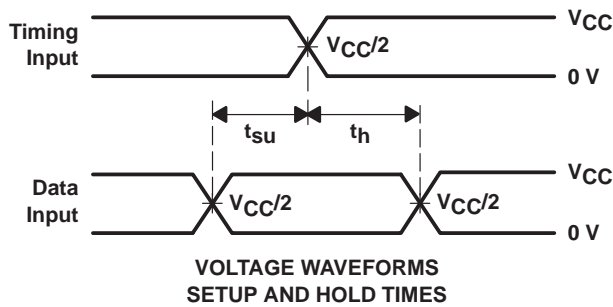
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PARAMETER MEASUREMENT INFORMATION
 $V_{CC} = 1.8\text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PHL}	GND

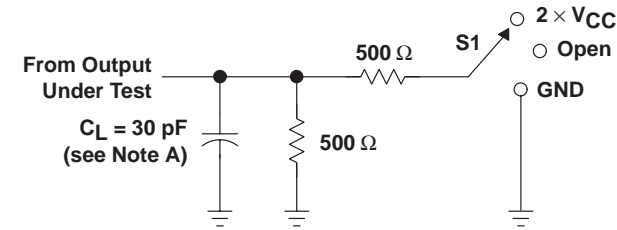


- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

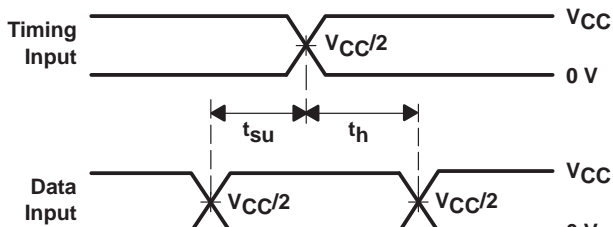
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$

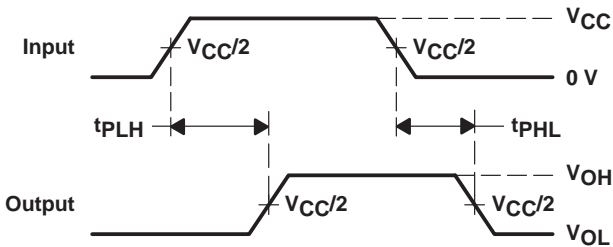


LOAD CIRCUIT

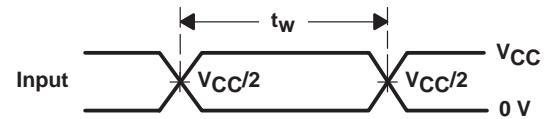
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND



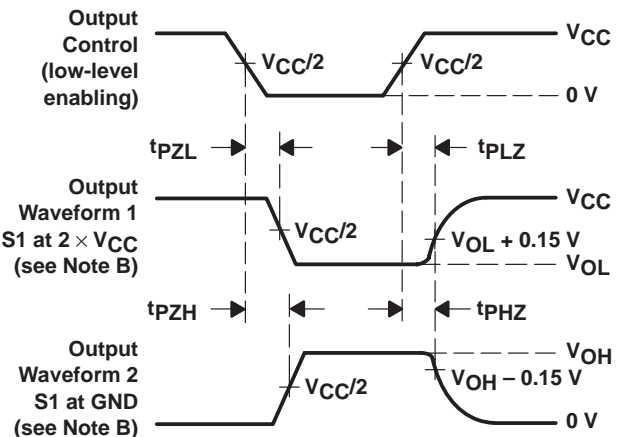
VOLTAGE WAVEFORMS
 SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
 PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
 PULSE DURATION



VOLTAGE WAVEFORMS
 ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .

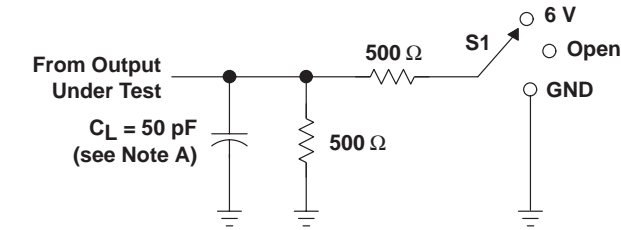
Figure 2. Load Circuit and Voltage Waveforms

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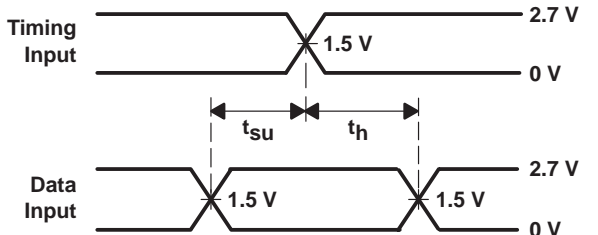
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$

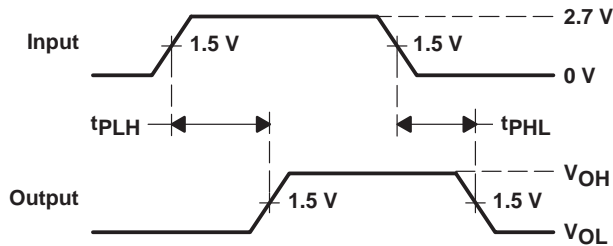


LOAD CIRCUIT

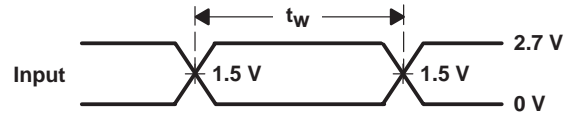
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



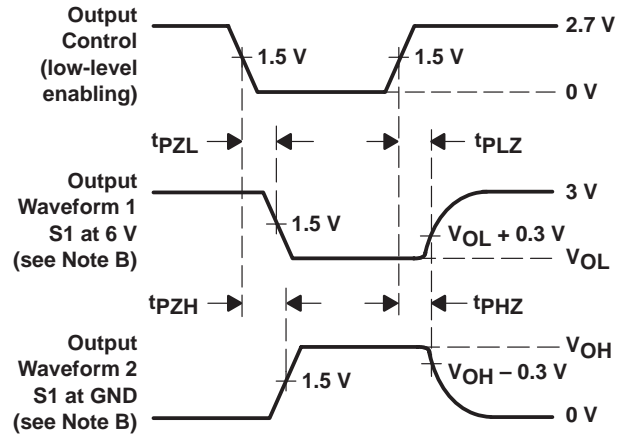
**VOLTAGE WAVEFORMS
 SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
 PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS
 PULSE DURATION**



**VOLTAGE WAVEFORMS
 ENABLE AND DISABLE TIMES**

- NOTES: A. C_L includes probe and jig capacitance.
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 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

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