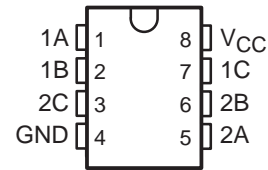
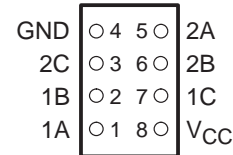


- Available in the Texas Instruments NanoStar™ and NanoFree™ Packages
- Operates at 0.8 V to 2.7 V
- Sub 1-V Operable
- Max t_{pd} of 0.5 ns at 1.8 V
- Low Power Consumption, 10 μ A at 2.7 V
- High On-Off Output Voltage Ratio
- High Degree of Linearity
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DCT OR DCU PACKAGE
(TOP VIEW)



YEP OR YZP PACKAGE
(BOTTOM VIEW)



description/ordering information

This dual analog switch is operational at 0.8-V to 2.7-V V_{CC} , but is designed specifically for 1.1-V to 2.7-V V_{CC} operation.

The SN74AUC2G66 can handle both analog and digital signals. It permits signals with amplitudes of up to 2.7-V (peak) to be transmitted in either direction.

NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
–40°C to 85°C	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YEP	Tape and reel	SN74AUC2G66YEPR	_ _ _ U6 _
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Tape and reel	SN74AUC2G66YZPR	_ _ _ U6 _
	SSOP – DCT	Tape and reel	SN74AUC2G66DCTR	U66 _ _ _
	VSSOP – DCU	Tape and reel	SN74AUC2G66DCUR	U66 _

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

‡ DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site.

DCU: The actual top-side marking has one additional character that designates the assembly/test site.

YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoStar and NanoFree are trademarks of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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SN74AUC2G66

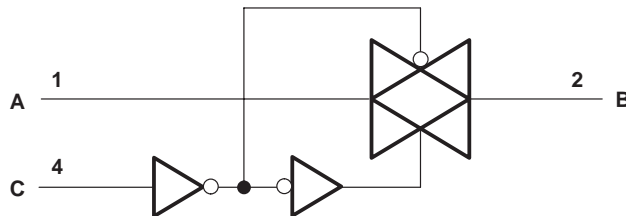
DUAL BILATERAL ANALOG SWITCH

SCES507 – NOVEMBER 2003

FUNCTION TABLE

CONTROL INPUT (C)	SWITCH
L	OFF
H	ON

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	-0.5 V to 3.6 V
Input voltage range, V_I (see Notes 1 and 2)	-0.5 V to 3.6 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Control input clamp current, I_{IK} ($V_I < 0$)	-50 mA
I/O port diode current, I_{IOK} ($V_{I/O} < 0$ or $V_{I/O} > V_{CC}$)	± 50 mA
On-state switch current, I_T ($V_{I/O} = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND	± 100 mA
Package thermal impedance, θ_{JA} (see Note 3):	
DCT package	220°C/W
DCU package	227°C/W
YEP/YZP package	102°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltages are with respect to ground unless otherwise specified.
 2. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	0.8	2.7	V
V _{IH}	High-level input voltage	V _{CC} = 0.8 V	V _{CC}	V
		V _{CC} = 1.1 V to 1.95 V	0.65 × V _{CC}	
		V _{CC} = 2.3 V to 2.7 V	1.7	
V _{IL}	Low-level input voltage	V _{CC} = 0.8 V	0	V
		V _{CC} = 1.1 V to 1.95 V	0.35 × V _{CC}	
		V _{CC} = 2.3 V to 2.7 V	0.7	
V _{I/O}	I/O port voltage	0	V _{CC}	V
V _I	Control input voltage	0	3.6	V
Δt/Δv	Input transition rise or fall rate	V _{CC} = 0.8 V to 1.65 V [†]	20	ns/V
		V _{CC} = 1.65 V to 2.3 V [‡]	20	
		V _{CC} = 2.3 V to 2.7 V [‡]	20	
T _A	Operating free-air temperature	-40	85	°C

[†] The data was taken at C_L = 15 pF, R_L = 2 kΩ (see Figure 1).

[‡] The data was taken at C_L = 30 pF, R_L = 500 Ω (see Figure 1).

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V _{CC}	MIN	TYP [§]	MAX	UNIT
r _{on}	On-state switch resistance	V _I = V _{CC} or GND, V _C = V _{IH} (see Figures 1 and 2)	I _S = 4 mA	1.1 V	17	40	Ω	
				1.65 V	7	20		
				2.3 V	4	15		
r _{on(p)}	Peak on resistance	V _I = V _{CC} to GND, V _C = V _{IH} (see Figures 1 and 2)	I _S = 4 mA	1.1 V	131	180	Ω	
				1.65 V	32	80		
				2.3 V	15	20		
Δr _{on}	Difference of on-state resistance between switches	V _I = V _{CC} to GND, V _C = V _{IH} (see Figures 1 and 2)	I _S = 4 mA	1.1 V		3	Ω	
				1.65 V		1		
				2.3 V		1		
I _{S(off)}	Off-state switch leakage current	V _I = V _{CC} and V _O = GND, or V _I = GND and V _O = V _{CC} , V _C = V _{IL} (see Figure 3)		2.7 V		±1	μA	
I _{S(on)}	On-state switch leakage current	V _I = V _{CC} or GND, V _C = V _{IH} , V _O = Open (see Figure 4)		2.7 V		±1	μA	
I _I	Control input current	V _I = V _{CC} or GND		0 to 2.7 V		±5	μA	
I _{CC}	Supply current	V _I = V _{CC} or GND, I _O = 0		0.8 V to 2.7 V		10	μA	
C _{ic}	Control input capacitance			2.5 V		2.5	pF	
C _{io(off)}	Switch input/output capacitance			2.5 V		3	pF	
C _{io(on)}	Switch input/output capacitance			2.5 V		7	pF	

[§] T_A = 25°C

SN74AUC2G66

DUAL BILATERAL ANALOG SWITCH

SCES507 – NOVEMBER 2003

switching characteristics over recommended operating free-air temperature range, $C_L = 15 \text{ pF}$ (unless otherwise noted) (see Figure 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 0.8 \text{ V}$	$V_{CC} = 1.2 \text{ V} \pm 0.1 \text{ V}$		$V_{CC} = 1.5 \text{ V} \pm 0.1 \text{ V}$		$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$			$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
t_{pd}^\dagger	A or B	B or A	1	0.6		0.5		0.5			0.4		ns
t_{en}	C	A or B	5	0.5	3	0.5	2.1	0.5	0.9	1.6	0.5	1.4	ns
t_{dis}	C	A or B	5.3	0.5	4	0.5	3	0.5	2.6	3.3	0.5	2.7	ns

† The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).

switching characteristics over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$ (unless otherwise noted) (see Figure 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$			$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{pd}^\dagger	A or B	B or A	0.7			0.7		ns
t_{en}	C	A or B	0.5	1.6	2.7	0.5	2.3	ns
t_{dis}	C	A or B	0.5	2.7	3.4	0.5	2	ns

† The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).

analog switch characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	TYP	UNIT
Frequency response ‡ (switch ON)	A or B	B or A	$C_L = 50 \text{ pF}$, $R_L = 600 \Omega$, $f_{in} = \text{sine wave}$ (see Figure 6)	0.8 V	101	MHz
				1.1 V	150	
				1.4 V	175	
				1.65 V	250	
				2.3 V	400	
			$C_L = 5 \text{ pF}$, $R_L = 50 \Omega$, $f_{in} = \text{sine wave}$ (see Figure 6)	0.8 V	450	
				1.1 V	>500	
				1.4 V	>500	
				1.65 V	>500	
				2.3 V	>500	
Crosstalk § (between switches)	A or B	B or A	$C_L = 50 \text{ pF}$, $R_L = 600 \Omega$, $f_{in} = 1 \text{ MHz}$ (sine wave) (see Figure 7)	0.8 V	-60	dB
				1.1 V	-60	
				1.4 V	-60	
				1.65 V	-60	
				2.3 V	-60	
			$C_L = 5 \text{ pF}$, $R_L = 50 \Omega$, $f_{in} = 1 \text{ MHz}$ (sine wave) (see Figure 7)	0.8 V	-65	
				1.1 V	-65	
				1.4 V	-65	
				1.65 V	-65	
				2.3 V	-65	

‡ Adjust f_{in} voltage to obtain 0 dBm at output. Increase f_{in} frequency until dB meter reads -3 dB.

§ Adjust f_{in} voltage to obtain 0 dBm at input.



analog switch characteristics, $T_A = 25^\circ\text{C}$ (continued)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V _{CC}	TYP	UNIT
Crosstalk (control input to signal output)	C	A or B	$C_L = 50\text{ pF}$, $R_L = 600\ \Omega$, $f_{in} = 1\text{ MHz}$ (square wave) (see Figure 8)	0.8 V	9	mV
				1.1 V	14	
				1.4 V	15	
				1.65 V	16	
				2.3 V	20	
Feed-through attenuation [‡] (switch OFF)	A or B	B or A	$C_L = 50\text{ pF}$, $R_L = 600\ \Omega$, $f_{in} = 1\text{ MHz}$ (sine wave) (see Figure 9)	0.8 V	-50	dB
				1.1 V	-50	
				1.4 V	-50	
				1.65 V	-50	
				2.3 V	-50	
			$C_L = 5\text{ pF}$, $R_L = 50\ \Omega$, $f_{in} = 1\text{ MHz}$ (sine wave) (see Figure 9)	0.8 V	-60	
				1.1 V	-60	
				1.4 V	-60	
				1.65 V	-60	
				2.3 V	-60	
Sine-wave distortion	A or B	B or A	$C_L = 50\text{ pF}$, $R_L = 10\text{ k}\Omega$, $f_{in} = 1\text{ kHz}$ (sine wave) (see Figure 10)	0.8 V	7	%
				1.1 V	0.25 6	
				1.4 V	0.04	
				1.65 V	0.03	
				2.3 V	0.01	
	A or B	B or A	$C_L = 50\text{ pF}$, $R_L = 10\text{ k}\Omega$, $f_{in} = 10\text{ kHz}$ (sine wave) (see Figure 10)	0.8 V	3.7	
				1.1 V	0.4	
				1.4 V	0.04	
				1.65 V	0.02	
				2.3 V	0.02	

[‡] Adjust f_{in} voltage to obtain 0 dBm at input.

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	V _{CC} = 0.8 V	V _{CC} = 1.2 V	V _{CC} = 1.5 V	V _{CC} = 1.8 V	V _{CC} = 2.5 V	UNIT
		TYP	TYP	TYP	TYP	TYP	
C _{pd} Power dissipation capacitance	f = 10 MHz	2.5	2.5	2.5	2.5	2.5	pF

SN74AUC2G66 DUAL BILATERAL ANALOG SWITCH

SCE5507 – NOVEMBER 2003

PARAMETER MEASUREMENT INFORMATION

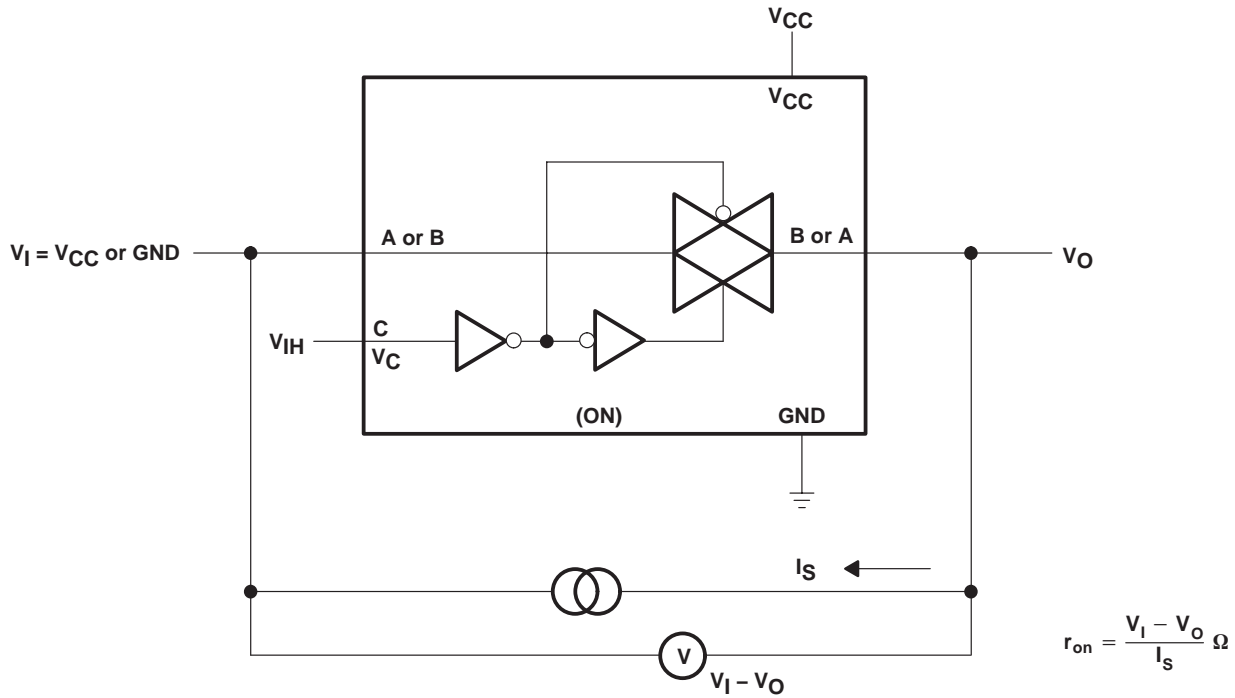


Figure 1. On-State Resistance Test Circuit

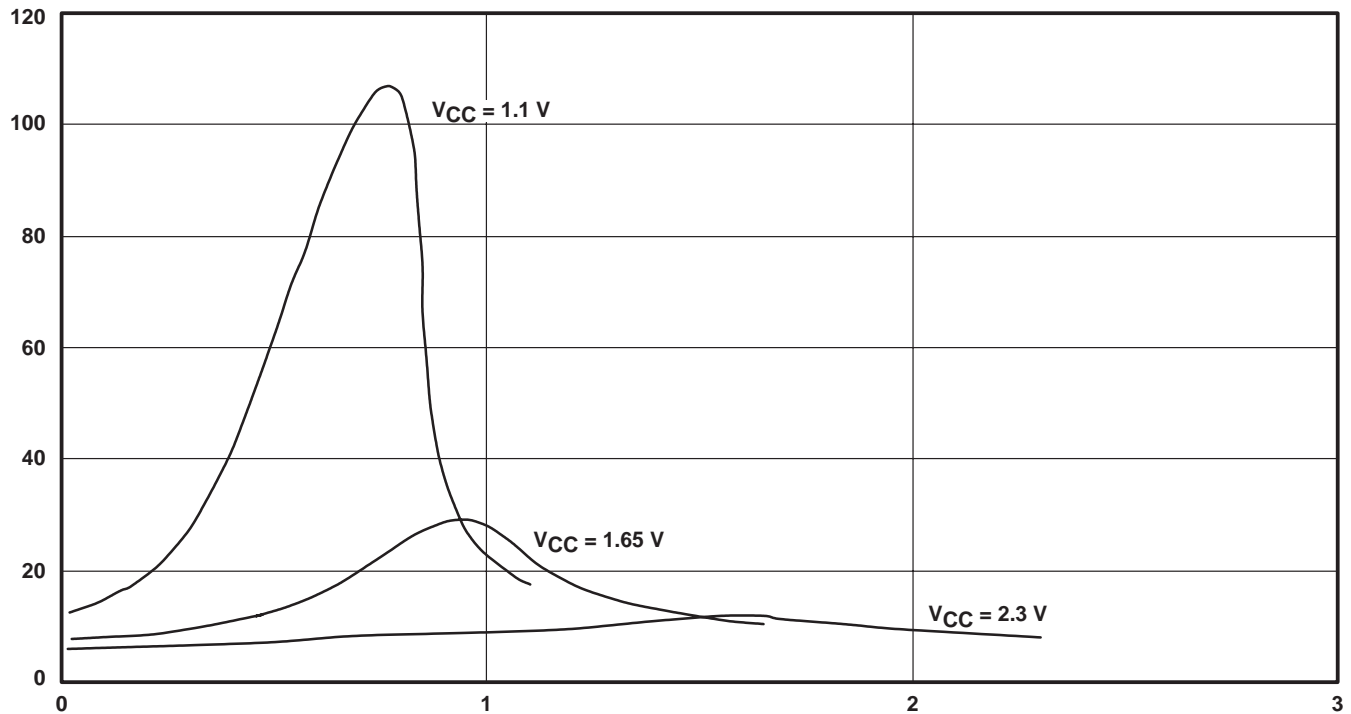


Figure 2. Typical r_{on} as a Function of Voltage (V_I) for $V_I = 0$ to V_{CC}

PARAMETER MEASUREMENT INFORMATION

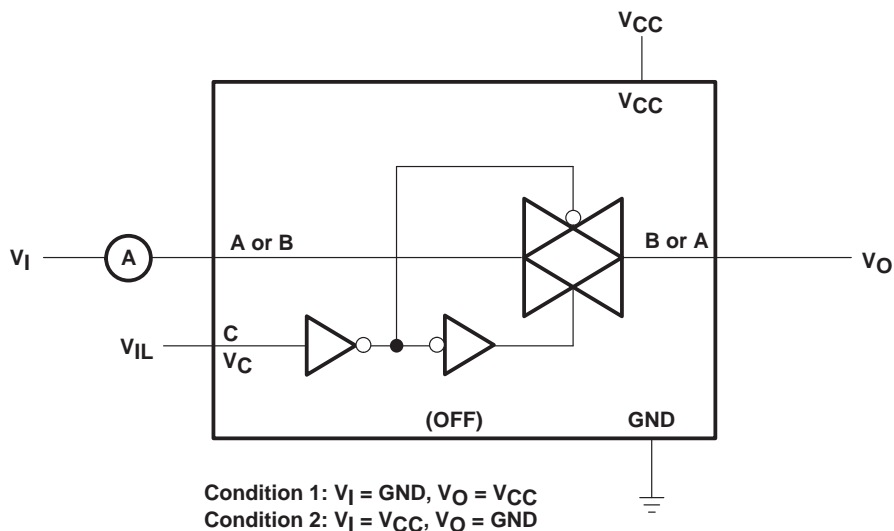


Figure 3. Off-State Switch Leakage-Current Test Circuit

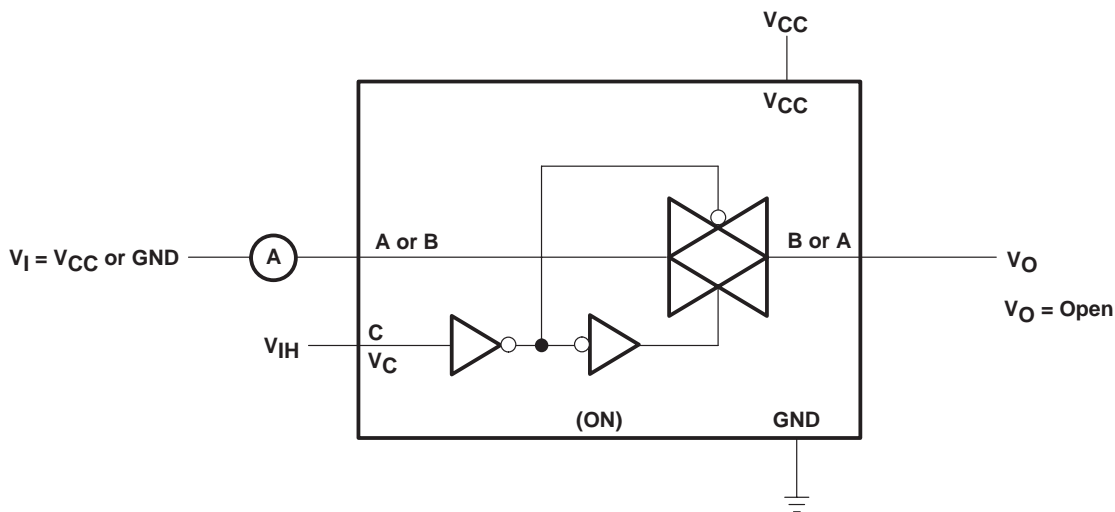
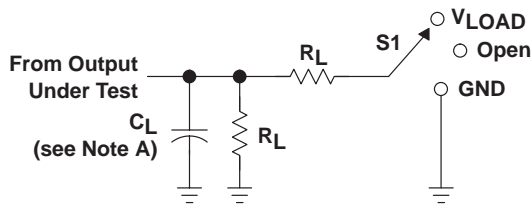


Figure 4. On-State Leakage-Current Test Circuit

SN74AUC2G66 DUAL BILATERAL ANALOG SWITCH

SCES507 – NOVEMBER 2003

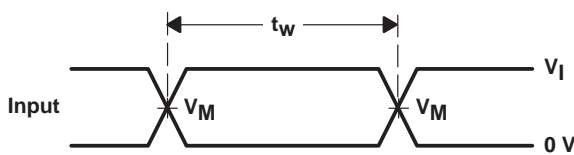
PARAMETER MEASUREMENT INFORMATION



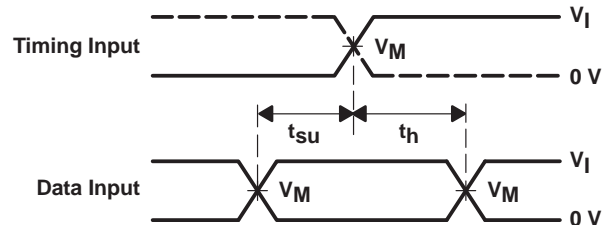
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT

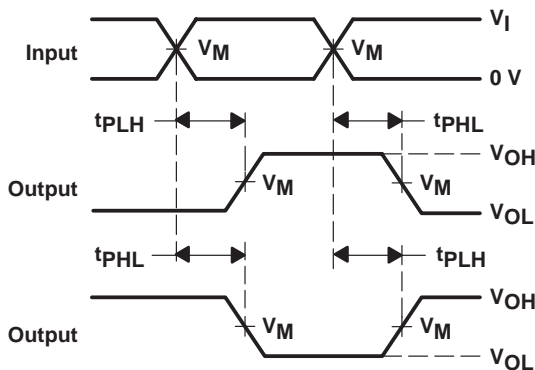
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
0.8 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 k Ω	0.1 V
$1.2 \text{ V} \pm 0.1 \text{ V}$	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 k Ω	0.1 V
$1.5 \text{ V} \pm 0.1 \text{ V}$	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 k Ω	0.1 V
$1.8 \text{ V} \pm 0.15 \text{ V}$	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 k Ω	0.15 V
$2.5 \text{ V} \pm 0.2 \text{ V}$	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 k Ω	0.15 V
$1.8 \text{ V} \pm 0.15 \text{ V}$	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5 \text{ V} \pm 0.2 \text{ V}$	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V



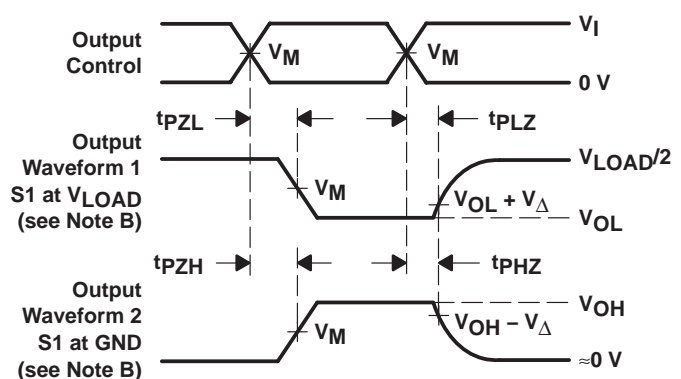
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, slew rate $\geq 1 \text{ V/ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 5. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

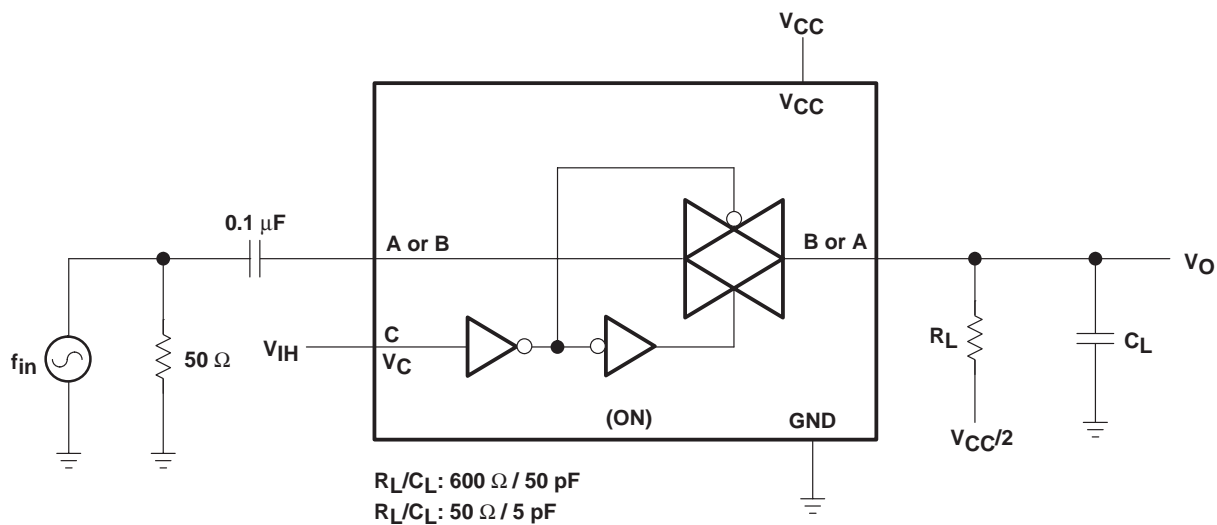


Figure 6. Frequency Response (Switch ON)

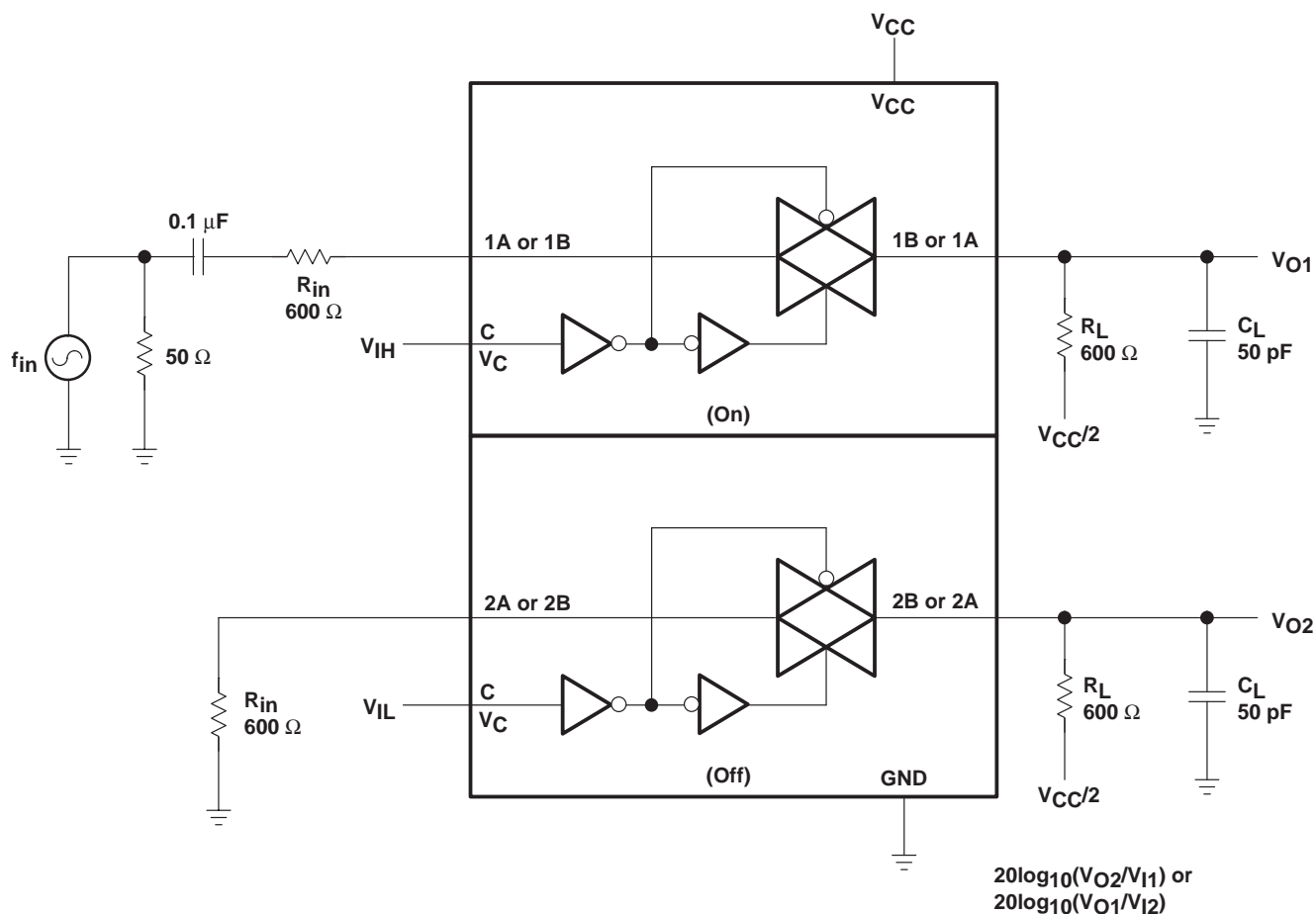


Figure 7. Crosstalk (Between Switches)

SN74AUC2G66 DUAL BILATERAL ANALOG SWITCH

SCES507 – NOVEMBER 2003

PARAMETER MEASUREMENT INFORMATION

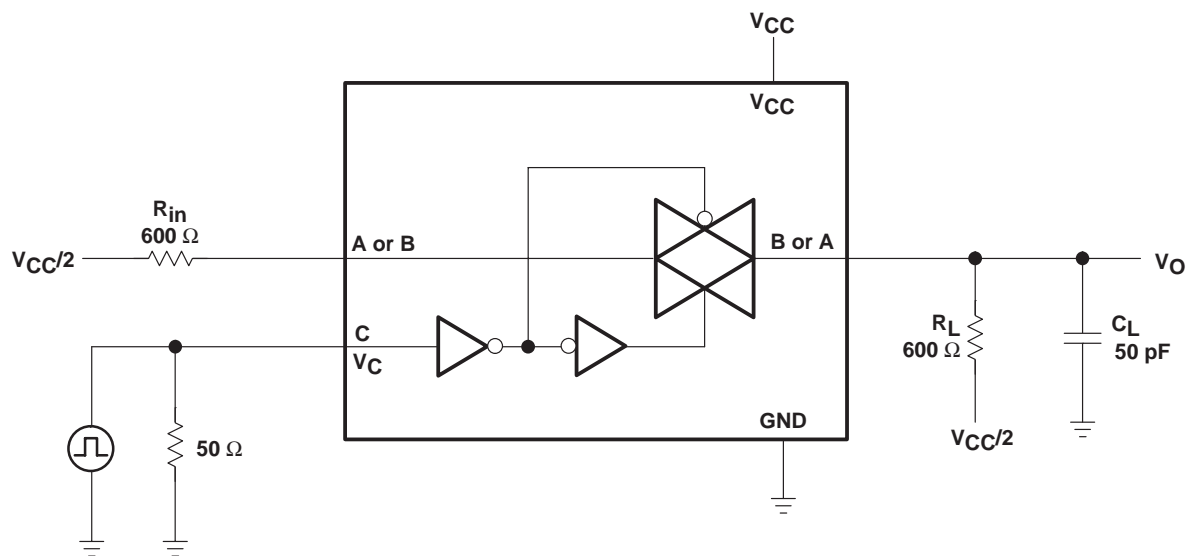


Figure 8. Crosstalk (Control Input – Switch Output)

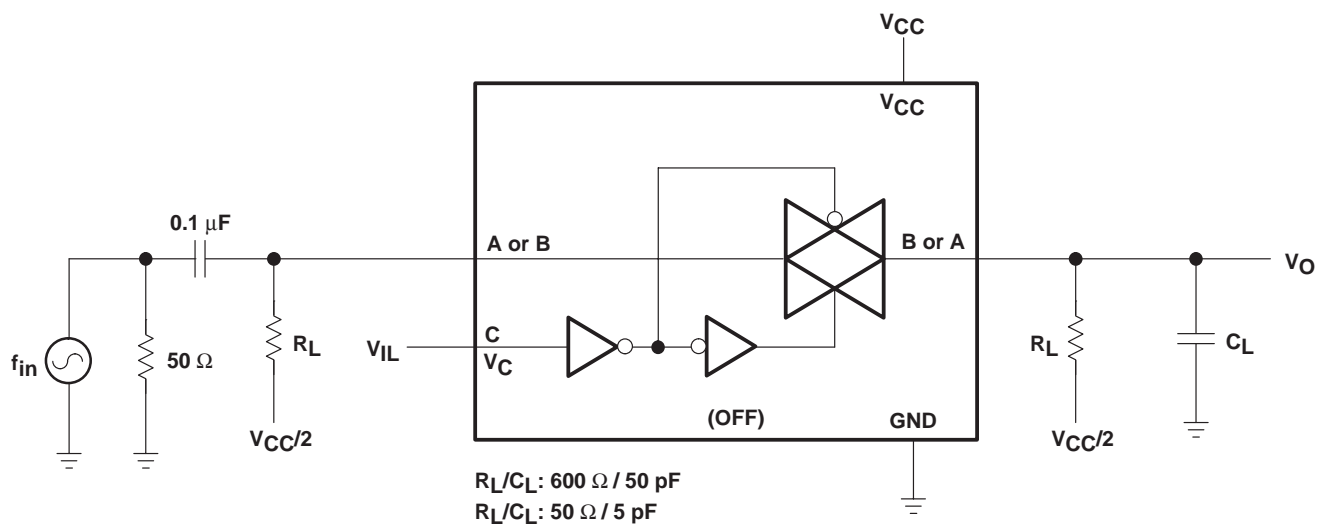


Figure 9. Feed Through, Switch Off

PARAMETER MEASUREMENT INFORMATION

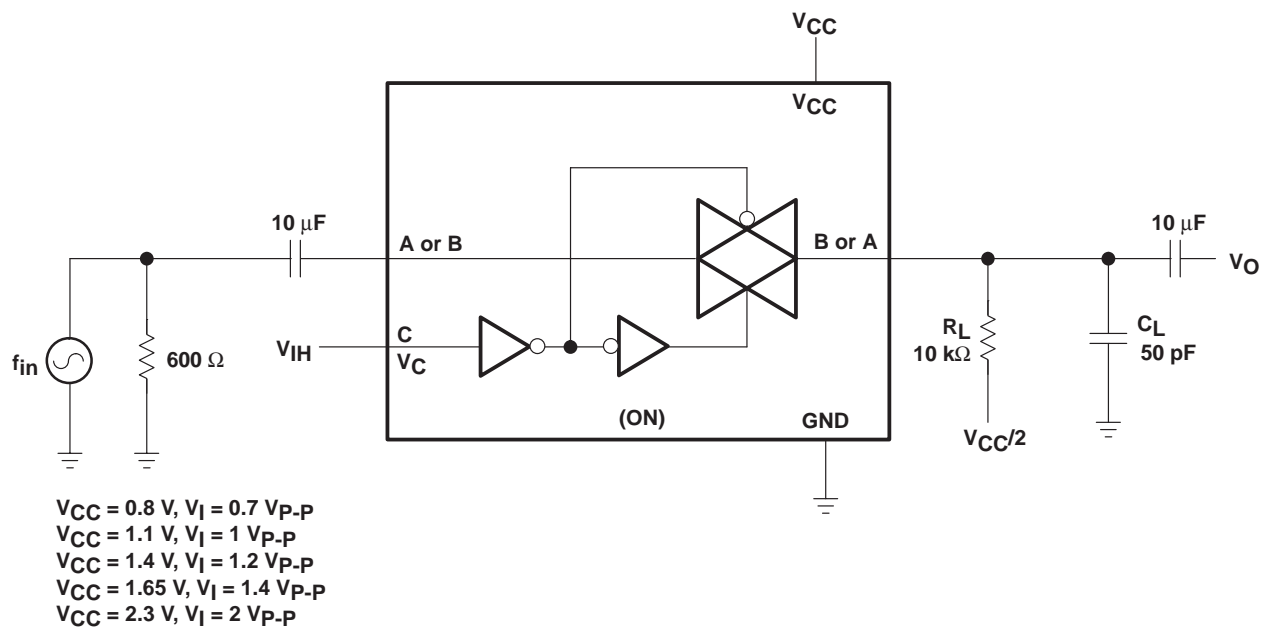
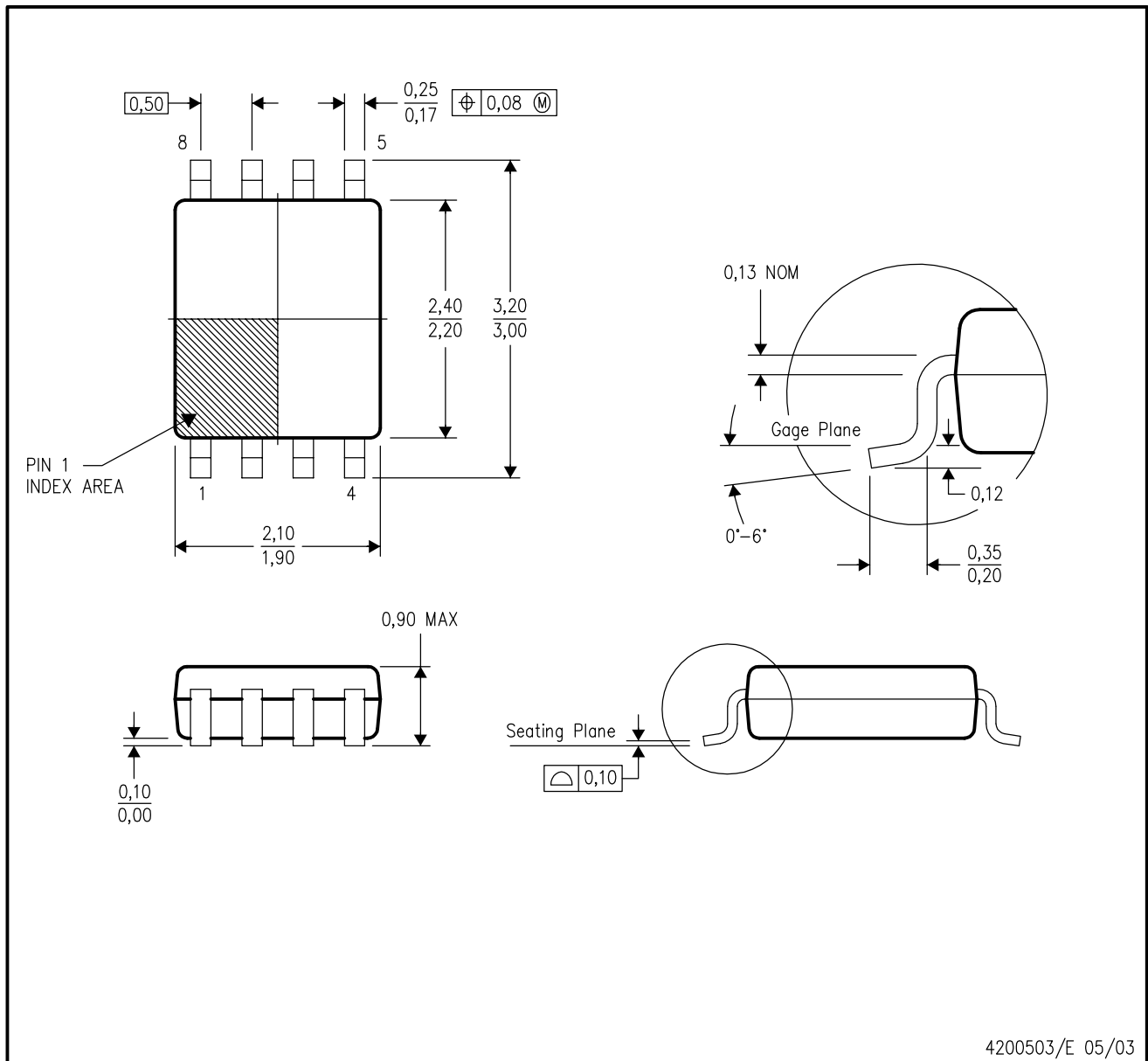


Figure 10. Sine-Wave Distortion

DCU (R-PDSO-G8)

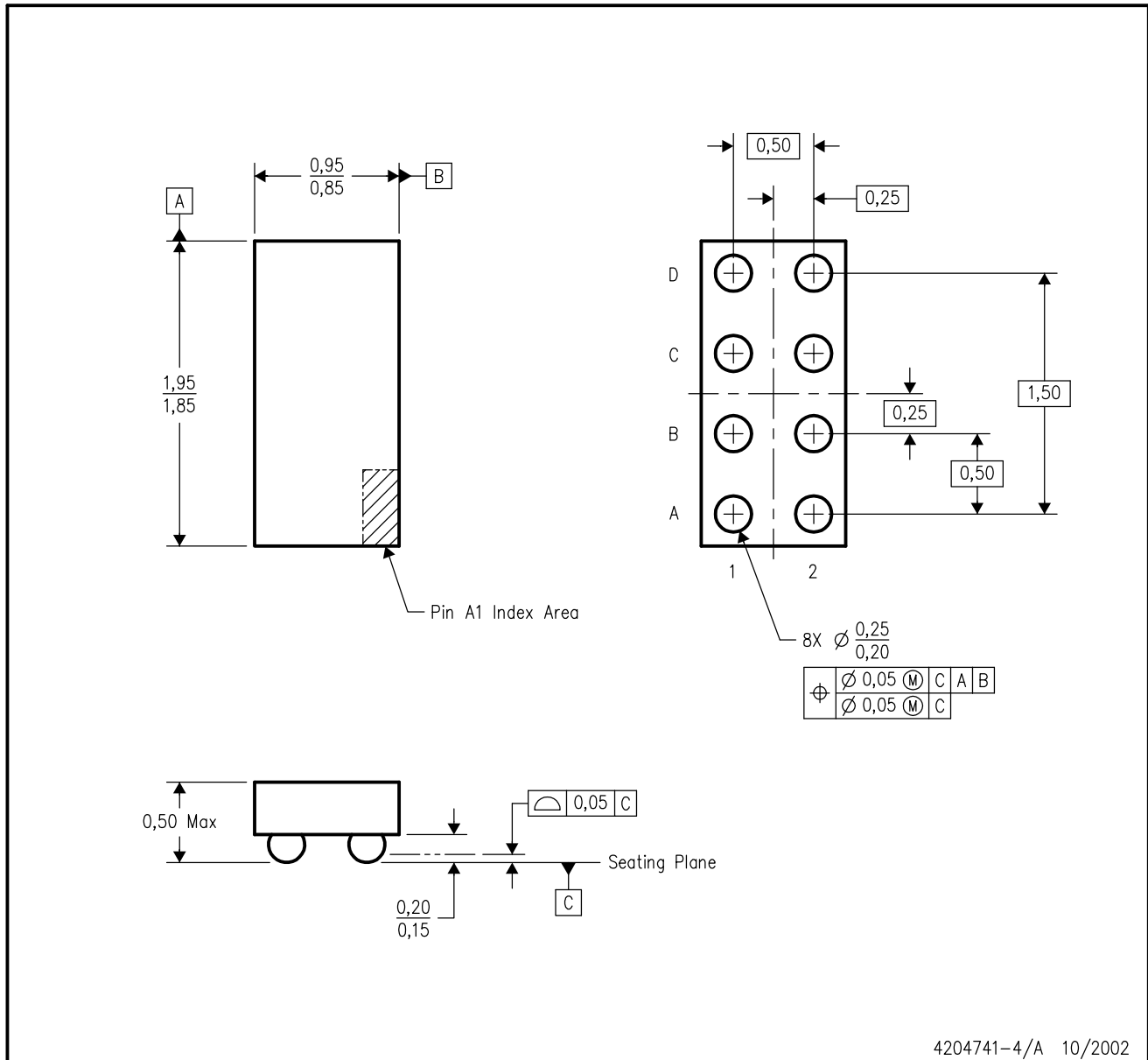
PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. Falls within JEDEC MO-187 variation CA.

YZP (R-XBGA-N8)

DIE-SIZE BALL GRID ARRAY

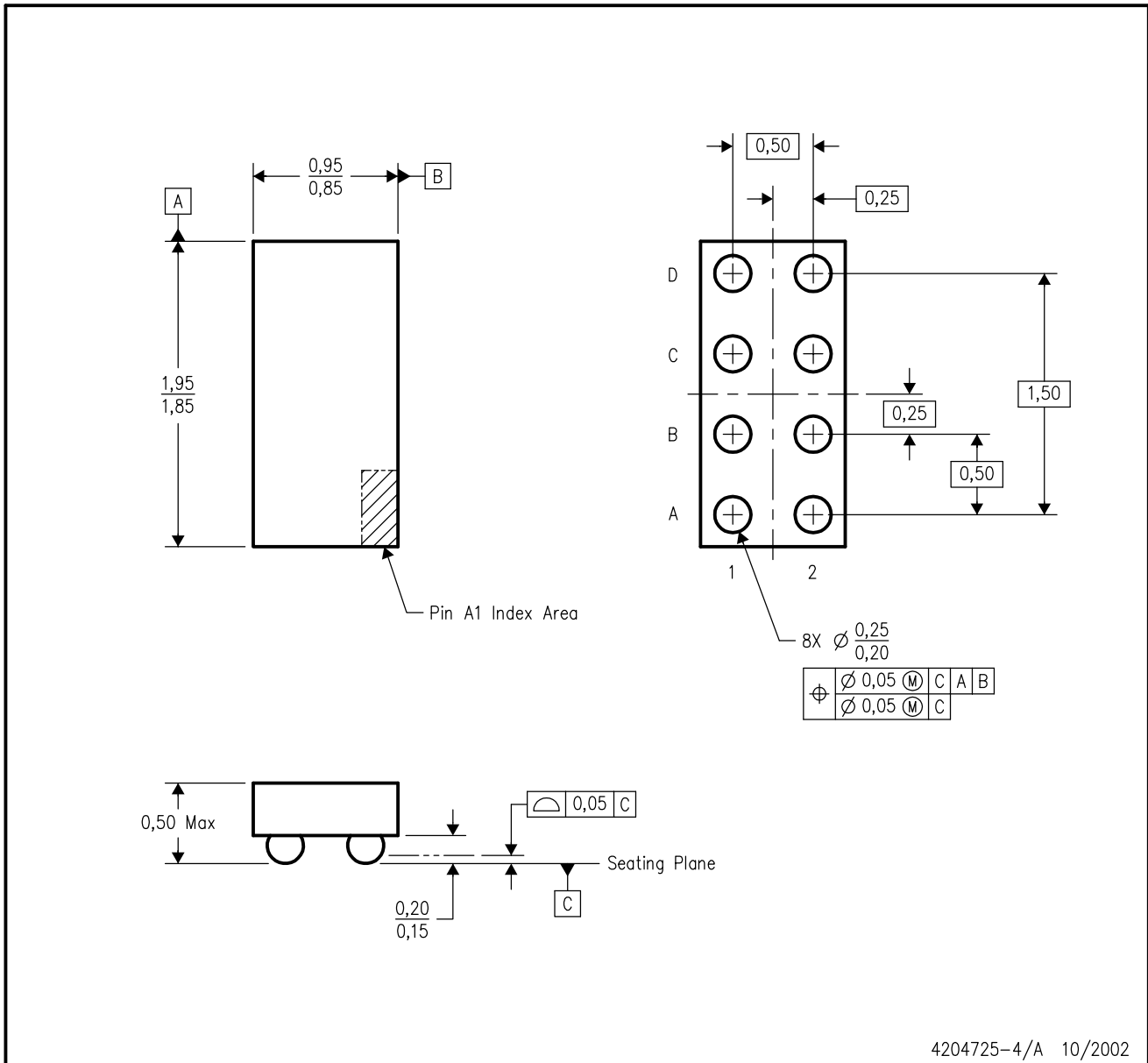


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 - D. This package is lead-free. Refer to the 8 YEP package (drawing 4204725) for tin-lead (SnPb).

NanoFree is a trademark of Texas Instruments.

YEP (R-XBGA-N8)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoStar™ package configuration.
 - D. This package is tin-lead (SnPb). Refer to the 8 YZP package (drawing 4204741) for lead-free.

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Mailing Address: Texas Instruments
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