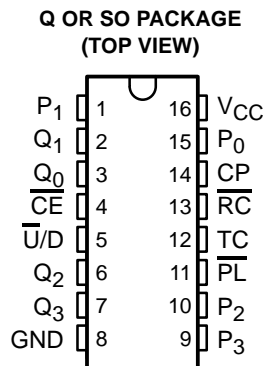


# CY74FCT191T 4-BIT UP/DOWN BINARY COUNTER

SCCS016A – MAY 1994 – REVISED SEPTEMBER 2001

- Function, Pinout, and Drive Compatible With FCT and F Logic
- Reduced  $V_{OH}$  (Typically = 3.3 V) Versions of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- Matched Rise and Fall Times
- 64-mA Output Sink Current  
32-mA Output Source Current



## description

The CY74FCT191T is a reversible modulo-16 binary counter, featuring synchronous counting and asynchronous presetting. The preset allows the CY74FCT191T to be used in programmable dividers. The count enable input, terminal count output, and ripple-clock output make possible a variety of methods of implementing multiusage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

### PIN DESCRIPTION

NAME	DESCRIPTION
$\overline{CE}$	Count enable input (active low)
CP	Clock pulse input (active rising edge)
P	Parallel data inputs
$\overline{PL}$	Asynchronous parallel load input (active low)
$\overline{U/D}$	Up/down count control input
Q	Flip-flop outputs
$\overline{RC}$	Ripple clock output (active low)
TC	Terminal count output



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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# CY74FCT191T

## 4-BIT UP/DOWN BINARY COUNTER

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### ORDERING INFORMATION

TA	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QSOP – Q	Tape and reel	6.2	CY74FCT191CTQCT	FT191-3
	SOIC – SO	Tube	6.2	CY74FCT191CTSOC	FCT191C
		Tape and reel	6.2	CY74FCT191CTSOCT	
	SOIC – SO	Tube	7.8	CY74FCT191ATSOC	FCT191A
		Tape and reel	7.8	CY74FCT191ATSOCT	


† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

### Function Tables

#### $\overline{RC}$ FUNCTION

INPUTS		OUTPUTS	
$\overline{CE}$	CP	TC†	$\overline{RC}$
L		H	
H	X	X	H
X	X	L	H

H = High logic level, L = Low logic level,

X = Don't care,  = Low pulse

† TC is generated internally.

#### MODE SELECT

INPUTS				MODE
$\overline{PL}$	$\overline{CE}$	$\overline{U/D}$	CP	
H	L	L	↑	Count up
H	L	H	↑	Count down
L	X	X	X	Preset (asynchronous)
H	H	X	X	No change (hold)

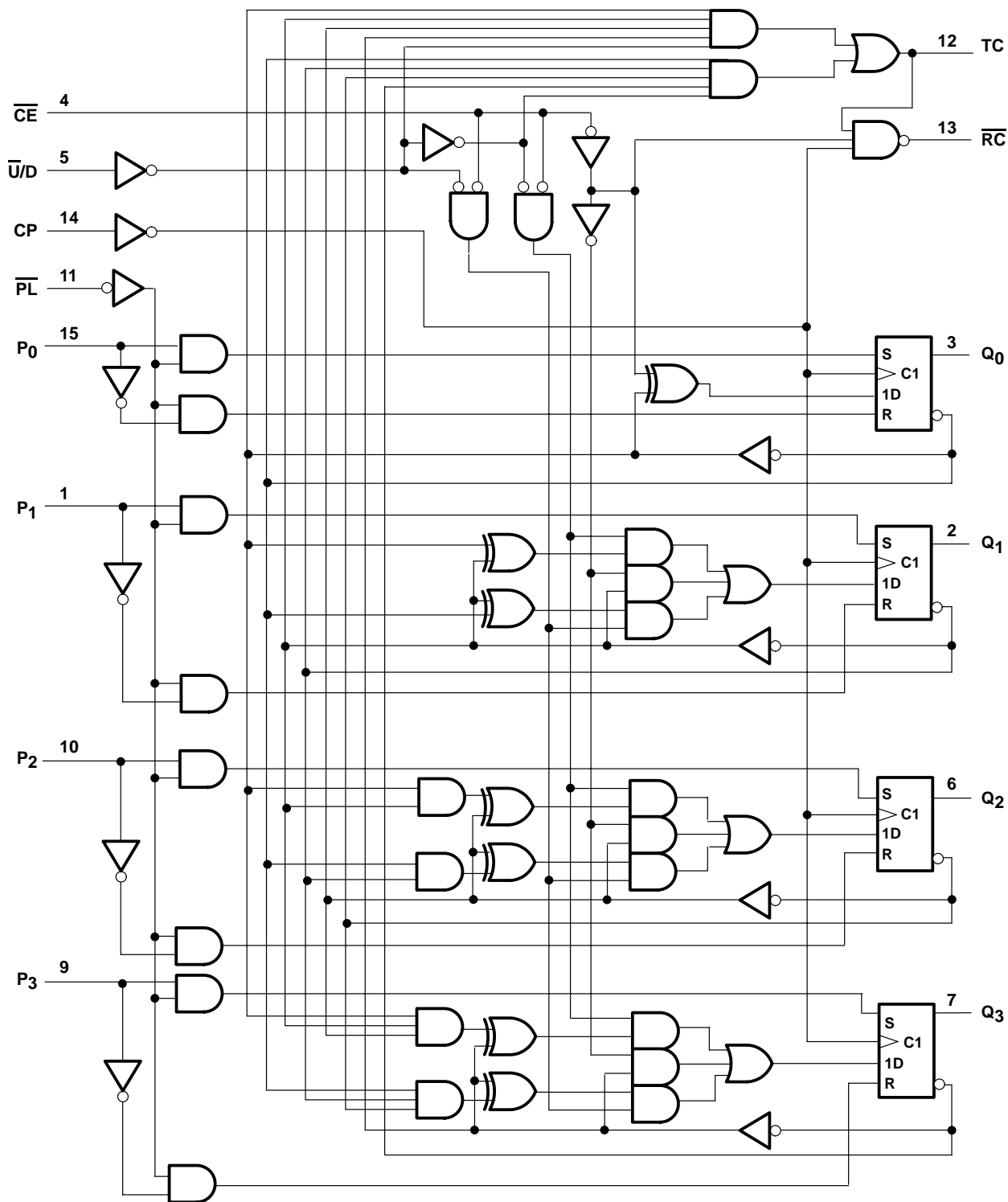
H = High logic level, L = Low logic level, X = Don't care,

↑ = Low-to-high clock transition

# CY74FCT191T 4-BIT UP/DOWN BINARY COUNTER

SCCS016A – MAY 1994 – REVISED SEPTEMBER 2001

logic diagram (positive logic)



# CY74FCT191T

## 4-BIT UP/DOWN BINARY COUNTER

SCCS016A – MAY 1994 – REVISED SEPTEMBER 2001

### absolute maximum rating over operating free-air temperature range (unless otherwise noted)†

Supply voltage range to ground potential	–0.5 V to 7 V
DC input voltage range	–0.5 V to 7 V
DC output voltage range	–0.5 V to 7 V
DC output current (maximum sink current/pin)	120 mA
Package thermal impedance, $\theta_{JA}$ (see Note 1): Q package	90°C/W
SO package	57°C/W
Ambient temperature range with power applied, $T_A$	–65°C to 135°C
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions (see Note 2)

	MIN	NOM	MAX	UNIT
$V_{CC}$ Supply voltage	4.75	5	5.25	V
$V_{IH}$ High-level input voltage	2			V
$V_{IL}$ Low-level input voltage			0.8	V
$I_{OH}$ High-level output current			–32	mA
$I_{OL}$ Low-level output current			64	mA
$T_A$ Operating free-air temperature	–40		85	°C

NOTE 2: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation.



# CY74FCT191T 4-BIT UP/DOWN BINARY COUNTER

SCCS016A – MAY 1994 – REVISED SEPTEMBER 2001

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V <sub>IK</sub>	V <sub>CC</sub> = 4.75 V,	I <sub>IN</sub> = -18 mA		-0.7	-1.2	V
V <sub>OH</sub>	V <sub>CC</sub> = 4.75 V,	I <sub>OH</sub> = -32 mA		2		V
	V <sub>CC</sub> = 4.75 V,	I <sub>OH</sub> = -15 mA	2.4	3.3		
V <sub>OL</sub>	V <sub>CC</sub> = 4.75 V,	I <sub>OL</sub> = 64 mA		0.3	0.55	V
V <sub>H</sub>	All inputs			0.2		V
I <sub>I</sub>	V <sub>CC</sub> = 5.25 V,	V <sub>IN</sub> = V <sub>CC</sub>			5	μA
I <sub>IH</sub>	V <sub>CC</sub> = 5.25 V,	V <sub>IN</sub> = 2.7 V			±1	μA
I <sub>IL</sub>	V <sub>CC</sub> = 5.25 V,	V <sub>IN</sub> = 0.5 V			±1	μA
I <sub>OS</sub> ‡	V <sub>CC</sub> = 5.25 V,	V <sub>OUT</sub> = 0 V	-60	-120	-225	mA
I <sub>off</sub>	V <sub>CC</sub> = 0 V,	V <sub>OUT</sub> = 4.5 V			±1	μA
I <sub>CC</sub>	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> ≤ 0.2 V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V			0.1	0.2	mA
ΔI <sub>CC</sub>	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = 3.4 V§, f <sub>1</sub> = 0, Outputs open			0.5	2	mA
I <sub>CCD</sub> ¶	V <sub>CC</sub> = 5.25 V, One bit switching at 50% duty cycle, Preset mode, Outputs open, MR = V <sub>CC</sub> = SR, PL = CE = U/D = CP = GND, V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V			0.06	0.12	mA/MHz
I <sub>C</sub> #	V <sub>CC</sub> = 5.25 V, Preset mode, Outputs open, PL = CE = U/D = CP = GND	One bit switching at f <sub>1</sub> = 5 MHz at 50% duty cycle	V <sub>IN</sub> = V <sub>CC</sub> or GND	0.4	0.8	mA
			V <sub>IN</sub> = 3.4 V or GND	0.7	1.8	mA
		Four bits switching at f <sub>1</sub> = 5 MHz at 50% duty cycle	V <sub>IN</sub> = V <sub>CC</sub> or GND	1.3	2.6	mA
			V <sub>IN</sub> = 3.4 V or GND	2.3	6.6	mA
C <sub>i</sub>				5	10	pF
C <sub>o</sub>				9	12	pF

† Typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

§ Per TTL-driven input (V<sub>IN</sub> = 3.4 V); all other inputs at V<sub>CC</sub> or GND

¶ This parameter is derived for use in total power-supply calculations.

# I<sub>C</sub> = I<sub>CC</sub> + ΔI<sub>CC</sub> × D<sub>H</sub> × N<sub>T</sub> + I<sub>CCD</sub> (f<sub>0</sub>/2 + f<sub>1</sub> × N<sub>1</sub>)

Where:

I<sub>C</sub> = Total supply current

I<sub>CC</sub> = Power-supply current with CMOS input levels

ΔI<sub>CC</sub> = Power-supply current for a TTL high input (V<sub>IN</sub> = 3.4 V)

D<sub>H</sub> = Duty cycle for TTL inputs high

N<sub>T</sub> = Number of TTL inputs at D<sub>H</sub>

I<sub>CCD</sub> = Dynamic current caused by an input transition pair (HLH or LHL)

f<sub>0</sub> = Clock frequency for registered devices, otherwise zero

f<sub>1</sub> = Input signal frequency

N<sub>1</sub> = Number of inputs changing at f<sub>1</sub>

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the I<sub>CC</sub> formula.



# CY74FCT191T

## 4-BIT UP/DOWN BINARY COUNTER

SCCS016A – MAY 1994 – REVISED SEPTEMBER 2001

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

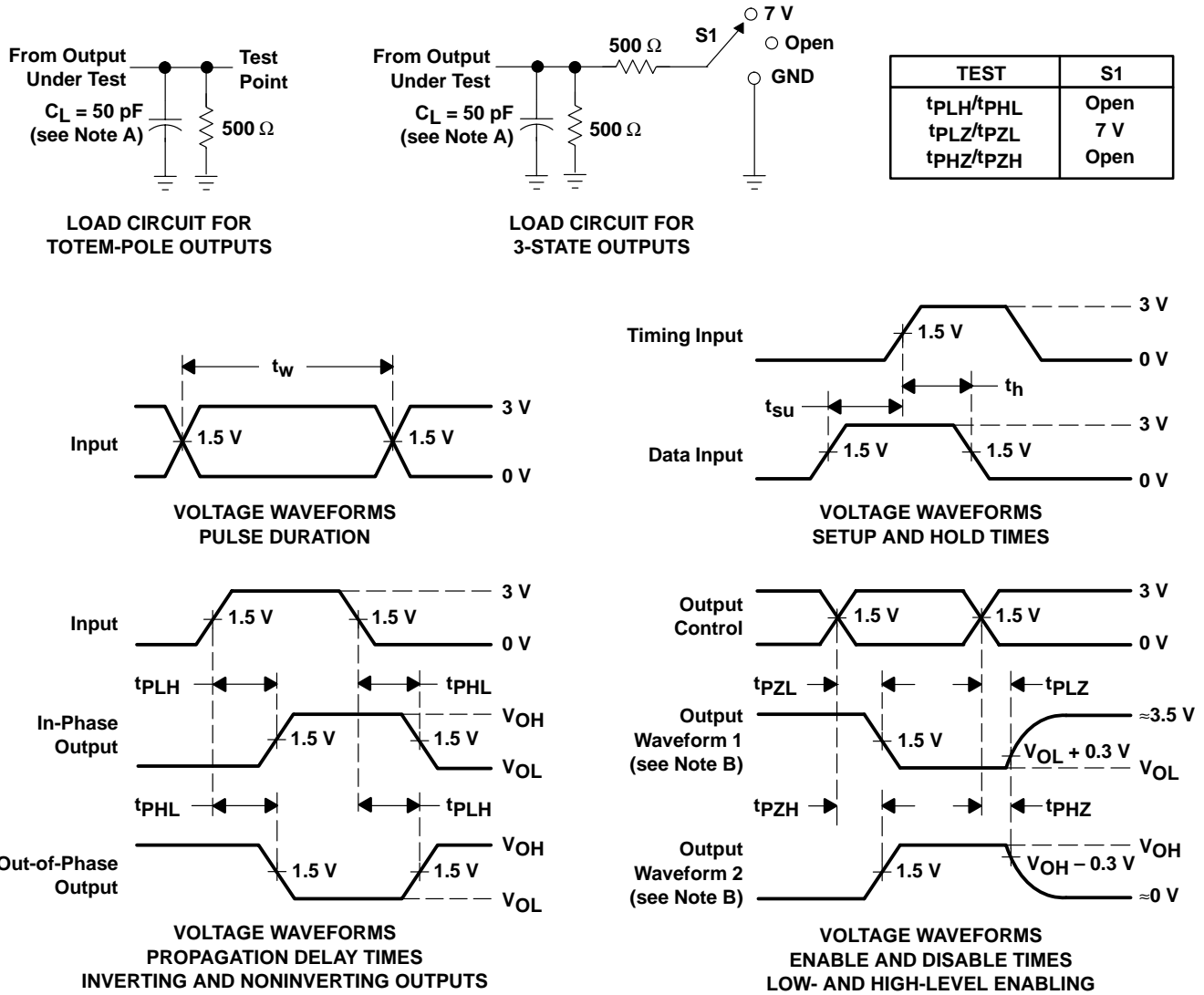
PARAMETER			CY74FCT191AT		CY74FCT191CT		UNIT
			MIN	MAX	MIN	MAX	
$t_w$	Pulse duration	CP	High or Low		4		ns
		$\overline{PL}$ low			5.5		
$t_{su}$	Setup time	Data before $\overline{PL}\downarrow$	High or Low		4		ns
		$\overline{CE}$ before $CP\uparrow$	Low		9		
		$\overline{U/D}$ before $CP\uparrow$	High or Low		10		
$t_h$	Hold time	Data after $\overline{PL}\downarrow$	High or Low		1.5		ns
		$\overline{CE}$ after $CP\uparrow$	Low		0		
		$\overline{U/D}$ after $CP\uparrow$	High or Low		0		
$t_{rec}$	Recovery time	$\overline{PL}$ after $CP\uparrow$			5		ns

switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY74FCT191AT		CY74FCT191CT		UNIT
			MIN	MAX	MIN	MAX	
$t_{PLH}$	CP	$Q_n$	1.5	7.8	1.5	6.2	ns
$t_{PHL}$			1.5	7.8	1.5	6.2	
$t_{PLH}$	CP	TC	1.5	11.8	1.5	9.4	ns
$t_{PHL}$			1.5	11.8	1.5	9.4	
$t_{PLH}$	CP	$\overline{RC}$	1.5	8.5	1.5	6.8	ns
$t_{PHL}$			1.5	8.5	1.5	6.8	
$t_{PLH}$	CE	$\overline{RC}$	1.5	7.2	1.5	6	ns
$t_{PHL}$			1.5	7.2	1.5	6	
$t_{PLH}$	$\overline{U/D}$	$\overline{RC}$	1.5	13	1.5	11	ns
$t_{PHL}$			1.5	13	1.5	11	
$t_{PLH}$	$\overline{U/D}$	TC	1.5	7.2	1.5	6.1	ns
$t_{PHL}$			1.5	7.2	1.5	6.1	
$t_{PLH}$	$P_n$	$Q_n$	1.5	9.1	1.5	7.7	ns
$t_{PHL}$			1.5	9.1	1.5	7.7	
$t_{PLH}$	$\overline{PL}$	$Q_n$	2	8.5	2	7.2	ns
$t_{PHL}$			2	8.5	2	7.2	



PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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### Mailing Address:

Texas Instruments  
Post Office Box 655303  
Dallas, Texas 75265