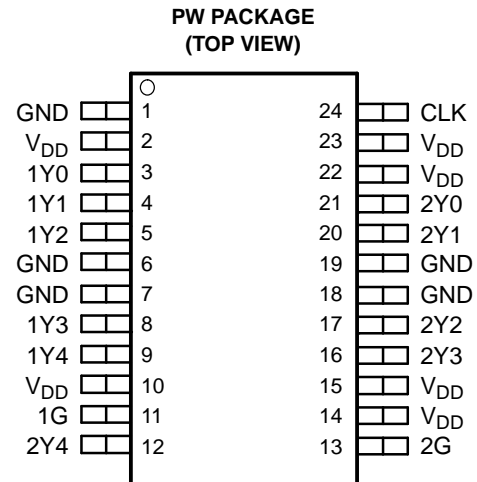


2.5-V TO 3.3-V HIGH-PERFORMANCE CLOCK BUFFER

- **High-Performance 1:10 Clock Driver for General-Purpose Applications. Operates up to 200 MHz at V_{DD} 3.3 V**
- **Pin-to-Pin Skew < 100 ps at V_{DD} 3.3 V**
- **V_{DD} Range: 2.3 V to 3.6 V**
- **Operating Temperature Range -40°C to 85°C**
- **Output Enable Glitch Suppression**
- **Distributes One Clock Input to Two Banks of Five Outputs**
- **25- Ω On-Chip Series Damping Resistors**
- **Packaged in 24-Pin TSSOP**



DESCRIPTION

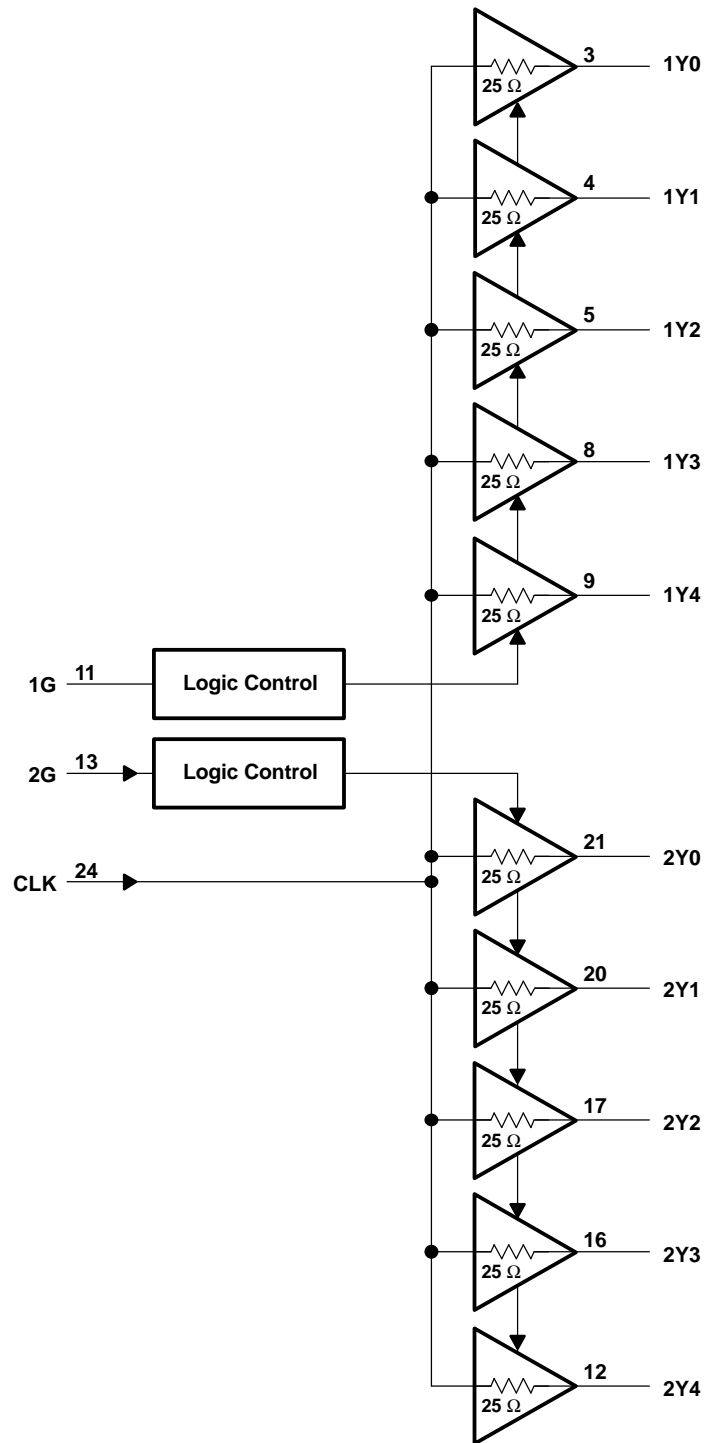
The CDCVF2310 is a high-performance, low-skew clock buffer that operates up to 200 MHz. Two banks of five outputs each provide low-skew copies of CLK. After power up, the default state of the outputs is low regardless of the state of the control pins. For normal operation, the outputs of bank 1Y[0:4] or 2Y[0:4] can be placed in a low state when the control pins (1G or 2G, respectively) are held low and a negative clock edge is detected on the CLK input. The outputs of bank 1Y[0:4] or 2Y[0:4] can be switched into the buffer mode when the control pins (1G and 2G) are held high and a negative clock edge is detected on the CLK input. The device operates in a 2.5-V and 3.3-V environment. The built-in output enable glitch suppression ensures a synchronized output enable sequence to distribute full period clock signals.

The CDCVF2310 is characterized for operation from -40°C to 85°C .



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

FUNCTIONAL BLOCK DIAGRAM



FUNCTION TABLE

INPUT			OUTPUT	
1G	2G	CLK	1Y[0:4]	2Y[0:4]
L	L	↓	L	L
H	L	↓	CLK ⁽¹⁾	L
L	H	↓	L	CLK ⁽¹⁾
H	H	↓	CLK ⁽¹⁾	CLK ⁽¹⁾

- (1) After detecting one negative edge on the CLK input, the output follows the input CLK if the control pin is held high.

Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
1G	11	I	Output enable control for 1Y[0:4] outputs. This output enable is active-high, meaning the 1Y[0:4] clock outputs follow the input clock (CLK) if this pin is logic high.
2G	13	I	Output enable control for 2Y[0:4] outputs. This output enable is active-high, meaning the 2Y[0:4] clock outputs follow the input clock (CLK) if this pin is logic high.
1Y[0:4]	3, 4, 5, 8, 9	O	Buffered output clocks
2Y[0:4]	21, 20, 17, 16, 12	O	Buffered output clocks
CLK	24	I	Input reference frequency
GND	1, 6, 7, 18, 19		Ground
V _{DD}	2, 10, 14, 15, 22, 23		DC power supply, 2.3 V – 3.6 V

DETAILED DESCRIPTION

Output Enable Glitch Suppression Circuit

The purpose of the glitch suppression circuitry is to ensure the output enable sequence is synchronized with the clock input such that the output buffer is enabled or disabled on the next full period of the input clock (negative edge triggered by the input clock) (see Figure 1).

The G input must fulfill the timing requirements (t_{su} , t_h) according to the *Switching Characteristics* table for predictable operation.

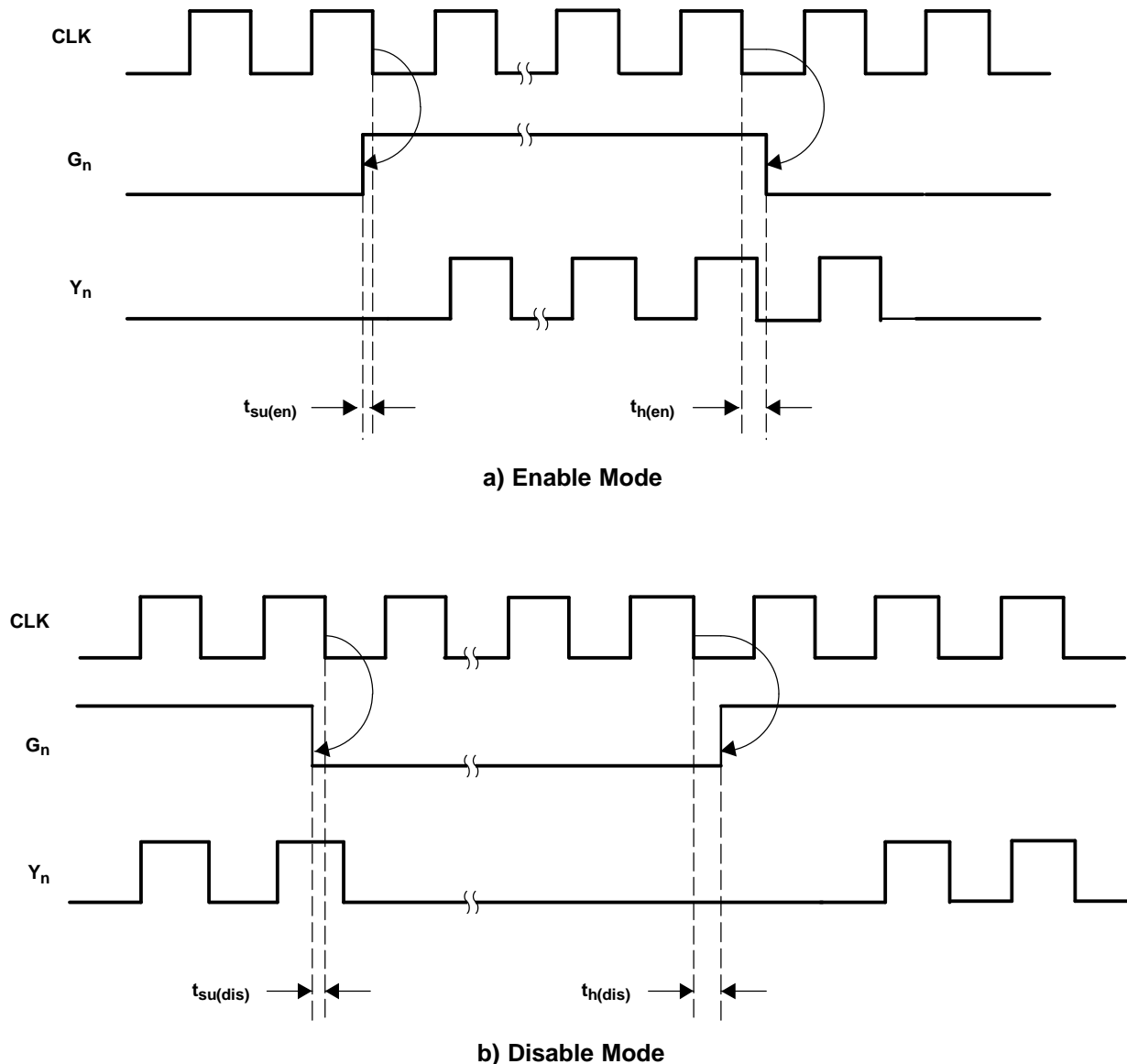


Figure 1. Enable and Disable Mode Relative to CLK↓

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

Supply voltage range, V_{DD}	–0.5 V to 4.6 V
Input voltage range, V_I ⁽²⁾⁽³⁾	–0.5 V to $V_{DD} + 0.5$ V
Output voltage range, V_O ⁽²⁾⁽³⁾	–0.5 V to $V_{DD} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$)	±50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$)	±50 mA
Continuous total output current, I_O ($V_O = 0$ to V_{DD})	±50 mA
Package thermal impedance, θ_{JA} ⁽⁴⁾ : PW package	120°C/W
Storage temperature range T_{stg}	–65°C to 150°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) This value is limited to 4.6 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51.

RECOMMENDED OPERATING CONDITIONS ⁽¹⁾

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		2.3	2.5		V
			3.3	3.6	
Low-level input voltage, V_{IL}	$V_{DD} = 3$ V to 3.6 V			0.8	V
	$V_{DD} = 2.3$ V to 2.7 V			0.7	
High-level input voltage, V_{IH}	$V_{DD} = 3$ V to 3.6 V	2			V
	$V_{DD} = 2.3$ V to 2.7 V	1.7			
Input voltage, V_I		0		V_{DD}	V
High-level output current, I_{OH}	$V_{DD} = 3$ V to 3.6 V			12	mA
	$V_{DD} = 2.3$ V to 2.7 V			6	
Low-level output current, I_{OL}	$V_{DD} = 3$ V to 3.6 V			12	mA
	$V_{DD} = 2.3$ V to 2.7 V			6	
Operating free-air temperature, T_A		–40		85	°C

- (1) Unused inputs must be held high or low to prevent them from floating.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
V_{IK}	Input voltage	$V_{DD} = 3$ V,	$I_I = -18$ mA			–1.2	V
I_I	Input current	$V_I = 0$ V or V_{DD}				±5	µA
I_{DD} ⁽²⁾	Static device current	CLK = 0 V or V_{DD} ,	$I_O = 0$ mA			80	µA
C_I	Input capacitance	$V_{DD} = 2.3$ V to 3.6 V,	$V_I = 0$ V or V_{DD}		2.5		pF
C_O	Output capacitance	$V_{DD} = 2.3$ V to 3.6 V,	$V_I = 0$ V or V_{DD}		2.8		pF

- (1) All typical values are at respective nominal V_{DD} .
- (2) For I_{CC} over frequency, see Figure 6.

V_{DD} = 3.3 V ±0.3 V

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}	High-level output voltage	V _{DD} = min to max,	I _{OH} = -100 µA	V _{DD} - 0.2			V
		V _{DD} = 3 V	I _{OH} = -12 mA	2.1			
			I _{OH} = -6 mA	2.4			
V _{OL}	Low-level output voltage	V _{DD} = min to max,	I _{OL} = -100 µA			0.2	V
		V _{DD} = 3 V	I _{OL} = 12 mA			0.8	
			I _{OL} = 6 mA			0.55	
I _{OH}	High-level output current	V _{DD} = 3 V,	V _O = 1 V	-28			mA
		V _{DD} = 3.3 V,	V _O = 1.65 V		-36		
		V _{DD} = 3.6 V,	V _O = 3.135 V			-14	
I _{OL}	Low-level output current	V _{DD} = 3 V,	V _O = 1.95 V	28			mA
		V _{DD} = 3.3 V,	V _O = 1.65 V		36		
		V _{DD} = 3.6 V,	V _O = 0.4 V			14	

(1) All typical values are at respective nominal V_{DD}.

V_{DD} = 2.5 V ±0.2 V

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}	High-level output voltage	V _{DD} = min to max,	I _{OH} = -100 µA	V _{DD} - 0.2			V
		V _{DD} = 2.3 V	I _{OH} = -6 mA	1.8			
V _{OL}	Low-level output voltage	V _{DD} = min to max,	I _{OL} = 100 µA			0.2	V
		V _{DD} = 2.3 V	I _{OL} = 6 mA			0.55	
I _{OH}	High-level output current	V _{DD} = 2.3 V,	V _O = 1 V	-17			mA
		V _{DD} = 2.5 V,	V _O = 1.25 V		-25		
		V _{DD} = 2.7 V,	V _O = 2.375 V			-10	
I _{OL}	Low-level output current	V _{DD} = 2.3 V,	V _O = 1.2 V	17			mA
		V _{DD} = 2.5 V,	V _O = 1.25 V		25		
		V _{DD} = 2.7 V,	V _O = 0.3 V			10	

(1) All typical values are at respective nominal V_{DD}.

TIMING REQUIREMENTS

over recommended ranges of supply voltage and operating free-air temperature

			MIN	NOM	MAX	UNIT
f _{clk}	Clock frequency	V _{DD} = 3 V to 3.6 V	0		200	MHz
		V _{DD} = 2.3 V to 2.7 V	0		170	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

$V_{DD} = 3.3\text{ V} \pm 0.3\text{ V}$ (SEE FIGURE 2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	CLK to Y_n	$f = 0\text{ MHz to }200\text{ MHz}$ For circuit load, see Figure 2.	1.3		2.8	ns
t_{PHL}						
$t_{sk(o)}$	Output skew (Y_m to Y_n) ⁽¹⁾ (see Figure 4)				100	ps
$t_{sk(p)}$	Pulse skew (see Figure 5)				250	ps
$t_{sk(pp)}$	Part-to-part skew				500	ps
t_r	Rise time (see Figure 3)	$V_O = 0.4\text{ V to }2\text{ V}$	0.7		2	V/ns
t_f	Fall time (see Figure 3)	$V_O = 2\text{ V to }0.4\text{ V}$	0.7		2	V/ns
$t_{su(en)}$	Enable setup time, G_{high} before CLK \downarrow		0.1			ns
$t_{su(dis)}$	Disable setup time, G_{low} before CLK \downarrow		0.1			ns
$t_{h(en)}$	Enable hold time, G_{high} after CLK \downarrow		0.4			ns
$t_{h(dis)}$	Disable hold time, G_{low} after CLK \downarrow		0.4			ns

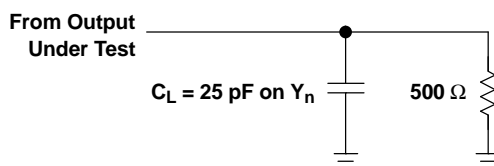
(1) The $t_{sk(o)}$ specification is only valid for equal loading of all outputs.

$V_{DD} = 2.5\text{ V} \pm 0.2\text{ V}$ (SEE FIGURE 2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	CLK to Y_n	$f = 0\text{ MHz to }170\text{ MHz}$ For circuit load, see Figure 2.	1.5		3.5	ns
t_{PHL}						
$t_{sk(o)}$	Output skew (Y_m to Y_n) ⁽¹⁾ (see Figure 4)				170	ps
$t_{sk(p)}$	Pulse skew (see Figure 5)				400	ps
$t_{sk(pp)}$	Part-to-part skew				600	ps
t_r	Rise time (see Figure 3)	$V_O = 0.4\text{ V to }1.7\text{ V}$	0.5		1.4	V/ns
t_f	Fall time (see Figure 3)	$V_O = 1.7\text{ V to }0.4\text{ V}$	0.5		1.4	V/ns
$t_{su(en)}$	Enable setup time, G_{high} before CLK \downarrow		0.1			ns
$t_{su(dis)}$	Disable setup time, G_{low} before CLK \downarrow		0.1			ns
$t_{h(en)}$	Enable hold time, G_{high} after CLK \downarrow		0.4			ns
$t_{h(dis)}$	Disable hold time, G_{low} after CLK \downarrow		0.4			ns

(1) The $t_{sk(o)}$ specification is only valid for equal loading of all outputs.

PARAMETER MEASUREMENT INFORMATION



- C_L includes probe and jig capacitance.
- All input pulses are supplied by generators having the following characteristics: $PRR \leq 200\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r < 1.2\text{ ns}$, $t_f < 1.2\text{ ns}$.

Figure 2. Test Load Circuit

PARAMETER MEASUREMENT INFORMATION (continued)

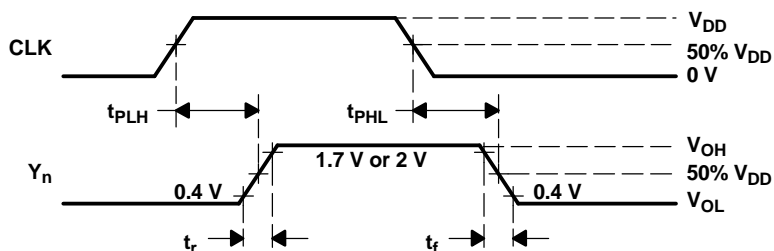


Figure 3. Voltage Waveforms Propagation Delay Times

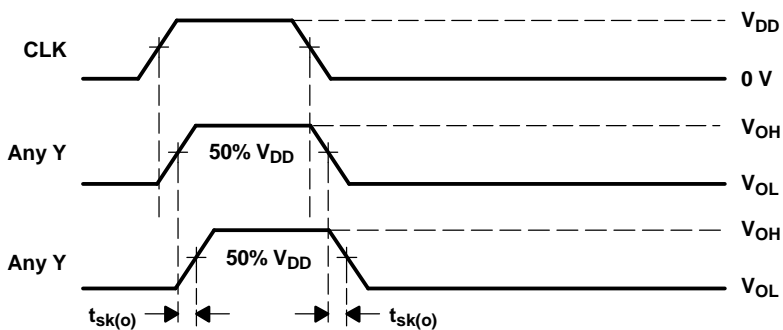
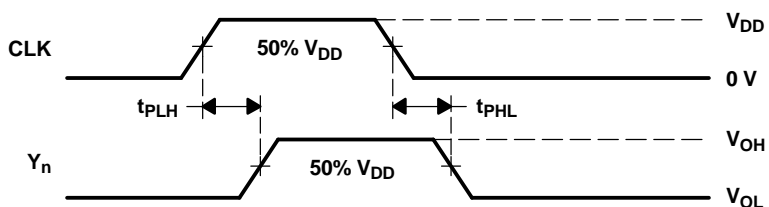


Figure 4. Output Skew



NOTE: $t_{sk(p)} = |t_{PLH} - t_{PHL}|$

Figure 5. Pulse Skew

PARAMETER MEASUREMENT INFORMATION (continued)

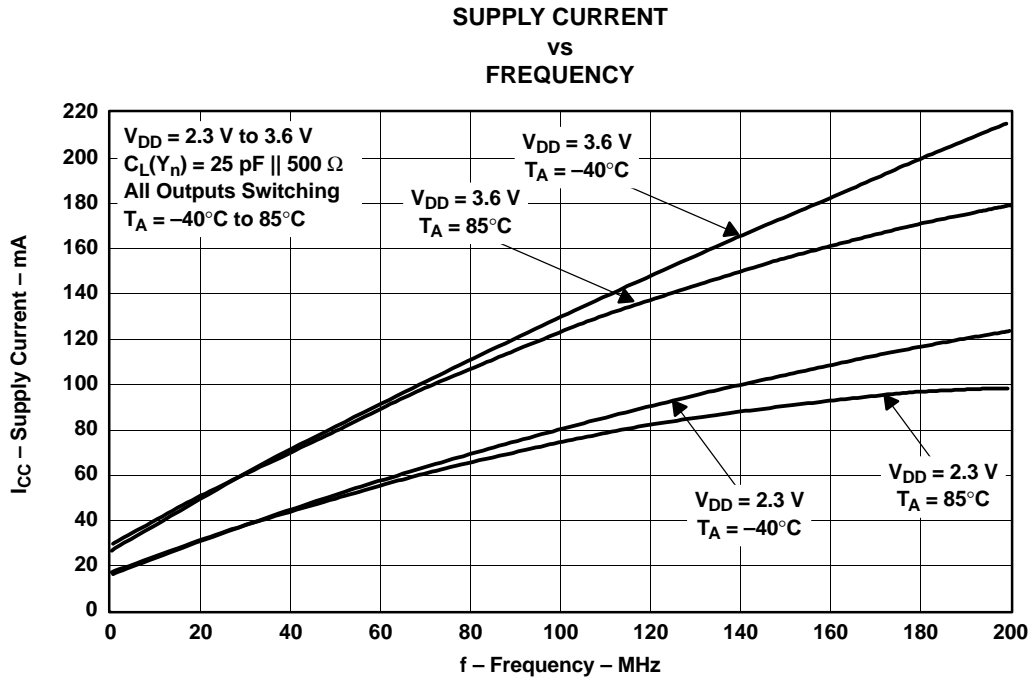


Figure 6.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265