

# CD4011UB Types

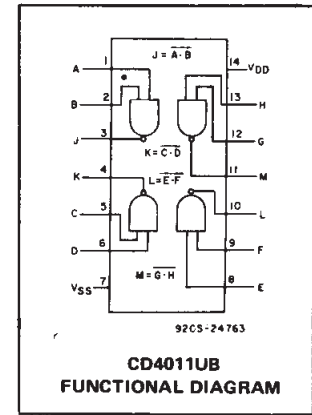
## CMOS Quad 2-Input NAND Gate High-Voltage Types (20-Volt Rating)

■ CD4011UB quad 2-input NAND gate provides the system designer with direct implementation of the NAND function and supplements the existing family of CMOS gates.

The CD4011UB types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

### Features:

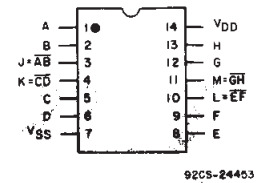
- Propagation delay time = 30 ns (typ.) at  $C_L = 50$  pF,  $V_{DD} = 10$  V
- Standardized symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1  $\mu$ A at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"



### MAXIMUM RATINGS, Absolute-Maximum Values:

|  |   |  |
|--|---|--|
| DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ )  | -0.5V to +20V                               |  |
| Voltages referenced to $V_{SS}$ Terminal                                     |   |  |
| INPUT VOLTAGE RANGE, ALL INPUTS  | -0.5V to $V_{DD} + 0.5$ V                   |  |
| DC INPUT CURRENT, ANY ONE INPUT  | $\pm 10$ mA                                 |  |
| POWER DISSIPATION PER PACKAGE ( $P_D$ ):                                     |   |  |
| For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$                        | 500mW                                       |  |
| For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$                       | Derate Linearly at 12mW/°C to 200mW         |  |
| DEVICE DISSIPATION PER OUTPUT TRANSISTOR                                     |   |  |
| FOR $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (All Package Types)               | 100mW                                       |  |
| OPERATING-TEMPERATURE RANGE ( $T_A$ )  | $-55^\circ\text{C}$ to $+125^\circ\text{C}$ |  |
| STORAGE TEMPERATURE RANGE ( $T_{stg}$ )                                      | $-65^\circ\text{C}$ to $+150^\circ\text{C}$ |  |
| LEAD TEMPERATURE (DURING SOLDERING):   |   |  |
| At distance $1/16 \pm 1/32$ inch ( $1.59 \pm 0.79$ mm) from case for 10s max | $+265^\circ\text{C}$                        |  |

### TERMINAL ASSIGNMENT



**TOP VIEW  
CD4011UB**

### RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

| CHARACTERISTIC  | MIN. | MAX. | UNITS |
|---|------|------|-------|
| Supply Voltage Range (For $T_A =$ Full Package Temperature Range) | 3    | 18   | V     |

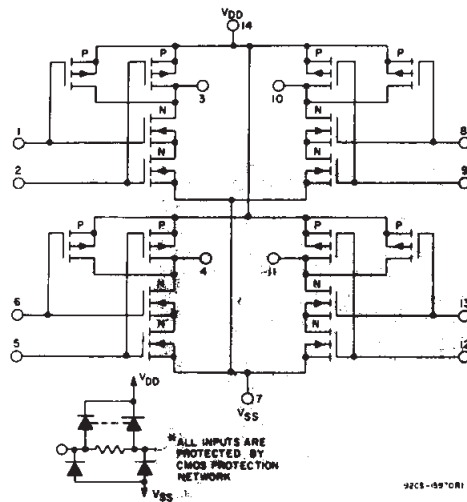


Fig. 1 - Schematic diagram for type CD4011UB.

# CD4011UB Types

## STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC                                     | CONDITIONS         |                     |                     | LIMITS AT INDICATED TEMPERATURES (°C) |       |       |       |       |                   |      | UNITS |
|--|--------------------|---------------------|---------------------|---------------------------------------|-------|-------|-------|-------|-------------------|------|-------|
|  | V <sub>O</sub> (V) | V <sub>IN</sub> (V) | V <sub>DD</sub> (V) |                                       |       |       |       | +25   |                   |      |       |
|  |                    |                     |                     | -55                                   | -40   | +85   | +125  | Min.  | Typ.              | Max. |       |
| Quiescent Device Current, I <sub>DD</sub> Max.     | -                  | 0,5                 | 5                   | 0.25                                  | 0.25  | 7.5   | 7.5   | -     | 0.01              | 0.25 | μA    |
|  | -                  | 0,10                | 10                  | 0.5                                   | 0.5   | 15    | 15    | -     | 0.01              | 0.5  |       |
|  | -                  | 0,15                | 15                  | 1                                     | 1     | 30    | 30    | -     | 0.01              | 1    |       |
|  | -                  | 0,20                | 20                  | 5                                     | 5     | 150   | 150   | -     | 0.02              | 5    |       |
| Output Low (Sink) Current I <sub>OL</sub> Min.     | 0.4                | 0,5                 | 5                   | 0.64                                  | 0.61  | 0.42  | 0.36  | 0.51  | 1                 | -    | mA    |
|  | 0.5                | 0,10                | 10                  | 1.6                                   | 1.5   | 1.1   | 0.9   | 1.3   | 2.6               | -    |       |
|  | 1.5                | 0,15                | 15                  | 4.2                                   | 4     | 2.8   | 2.4   | 3.4   | 6.8               | -    |       |
| Output High (Source) Current, I <sub>OH</sub> Min. | 4.6                | 0,5                 | 5                   | -0.64                                 | -0.61 | -0.42 | -0.36 | -0.51 | -1                | -    | mA    |
|  | 2.5                | 0,5                 | 5                   | -2                                    | -1.8  | -1.3  | -1.15 | -1.6  | -3.2              | -    |       |
|  | 9.5                | 0,10                | 10                  | -1.6                                  | -1.5  | -1.1  | -0.9  | -1.3  | -2.6              | -    |       |
| Output Voltage: Low-Level, V <sub>OL</sub> Max.    | -                  | 0,5                 | 5                   | 0.05                                  |       |       |       | -     | 0                 | 0.05 | V     |
|  | -                  | 0,10                | 10                  | 0.05                                  |       |       |       | -     | 0                 | 0.05 |       |
|  | -                  | 0,15                | 15                  | 0.05                                  |       |       |       | -     | 0                 | 0.05 |       |
| Output Voltage: High-Level, V <sub>OH</sub> Min.   | -                  | 0,5                 | 5                   | 4.95                                  |       |       |       | 4.95  | 5                 | -    | V     |
|  | -                  | 0,10                | 10                  | 9.95                                  |       |       |       | 9.95  | 10                | -    |       |
|  | -                  | 0,15                | 15                  | 14.95                                 |       |       |       | 14.95 | 15                | -    |       |
| Input Low Voltage, V <sub>IL</sub> Max.            | 4.5                | -                   | 5                   | 1                                     |       |       |       | -     | -                 | 1    | V     |
|  | 9                  | -                   | 10                  | 2                                     |       |       |       | -     | -                 | 2    |       |
|  | 13.5               | -                   | 15                  | 2.5                                   |       |       |       | -     | -                 | 2.5  |       |
| Input High Voltage, V <sub>IH</sub> Min.           | 0.5,4.5            | -                   | 5                   | 4                                     |       |       |       | 4     | -                 | -    | V     |
|  | 1,9                | -                   | 10                  | 8                                     |       |       |       | 8     | -                 | -    |       |
|  | 1.5,13.5           | -                   | 15                  | 12.5                                  |       |       |       | 12.5  | -                 | -    |       |
| Input Current I <sub>IN</sub> Max.                 |                    | 0,18                | 18                  | ±0.1                                  | ±0.1  | ±1    | ±1    | -     | ±10 <sup>-5</sup> | ±0.1 | μA    |

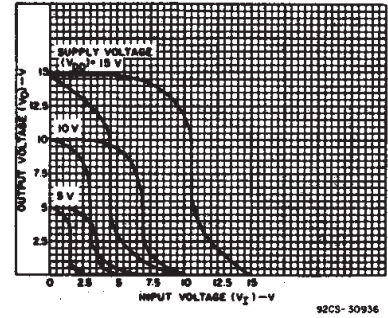


Fig. 2 - Minimum and maximum voltage transfer characteristics.

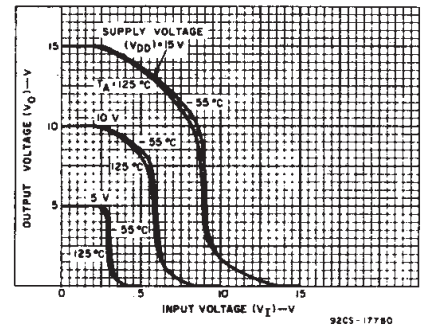


Fig. 3 - Typical voltage transfer characteristics as a function of temperature.

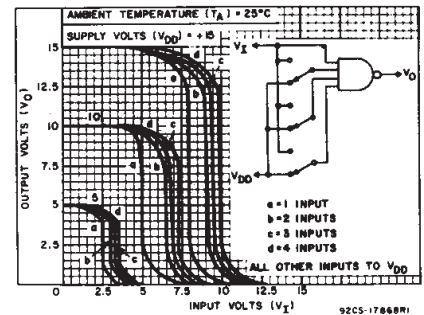


Fig. 4 - Typical multiple input switching transfer characteristics for CD4012UB.

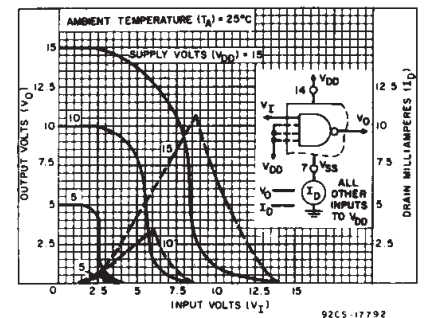


Fig. 5 - Typical current and voltage transfer characteristics.

## DYNAMIC ELECTRICAL CHARACTERISTICS

At  $T_A = 25^\circ\text{C}$ , Input  $t_p, t_f = 20\text{ ns}$ , and  $C_L = 50\text{ pF}$ ,  $R_L = 200\text{ k}\Omega$

| CHARACTERISTIC                             | TEST CONDITIONS | LIMITS                |      | UNITS |     |
|--|-----------------|-----------------------|------|-------|-----|
|  |                 | V <sub>DD</sub> VOLTS | TYP. |       | MAX |
| Propagation Delay Time, $t_{PHL}, t_{PLH}$ |                 | 5                     | 60   | 120   | ns  |
|  |                 | 10                    | 30   | 60    |     |
|  |                 | 15                    | 25   | 50    |     |
| Transition Time, $t_{THL}, t_{TLH}$        |                 | 5                     | 100  | 200   | ns  |
|  |                 | 10                    | 50   | 100   |     |
|  |                 | 15                    | 40   | 80    |     |
| Input Capacitance, C <sub>IN</sub>         | Any Input       |                       | 10   | 15    | pF  |

# CD4011UB Types

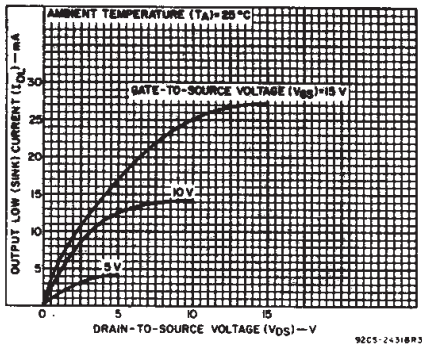


Fig. 6 - Typical output low (sink) current characteristics.

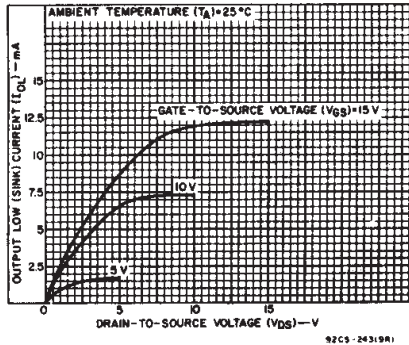


Fig. 7 - Minimum output low (sink) current characteristics.

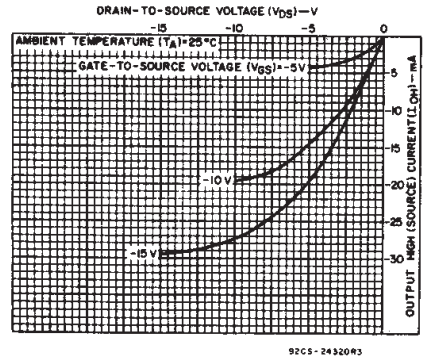


Fig. 8 - Typical output high (source) current characteristics.

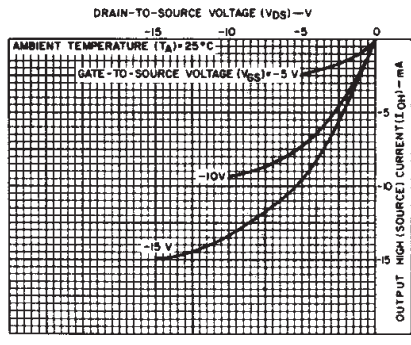


Fig. 9 - Minimum output high (source) current characteristics.

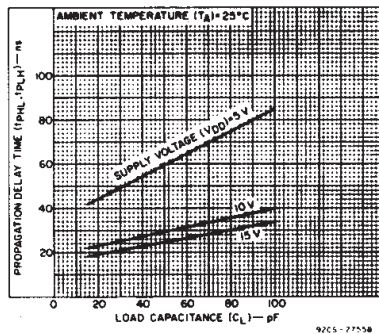


Fig. 10 - Typical propagation delay time vs. load capacitance.

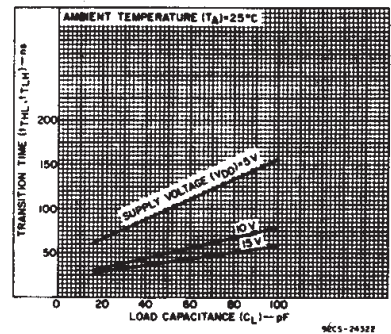


Fig. 11 - Typical transition time vs. load capacitance.

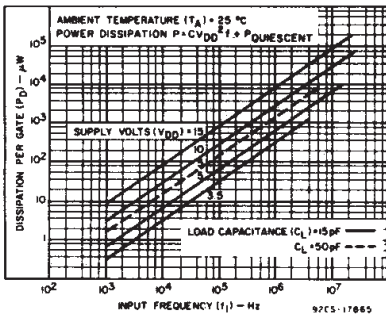


Fig. 12 - Typical power dissipation vs. frequency characteristics.

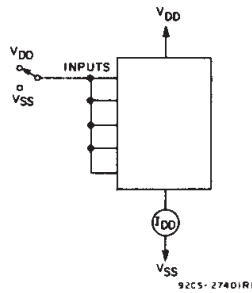
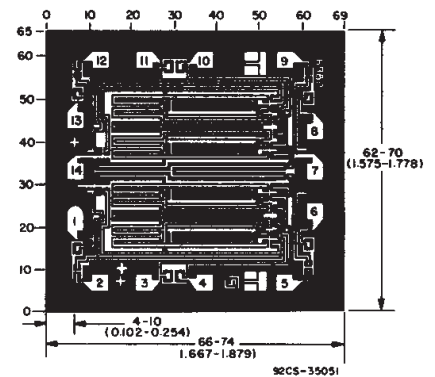


Fig. 13 - Quiescent device current test circuit.

## Chip Dimensions and Pad Layout



CD4011UBH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

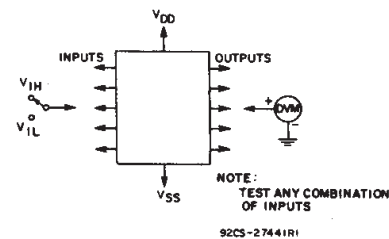


Fig. 14 - Input voltage test circuit.

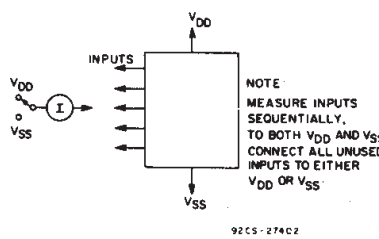
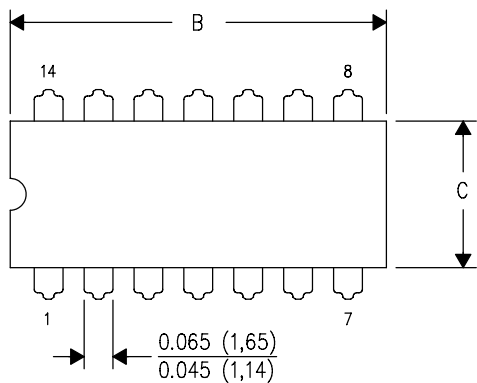


Fig. 15 - Input current test circuit.

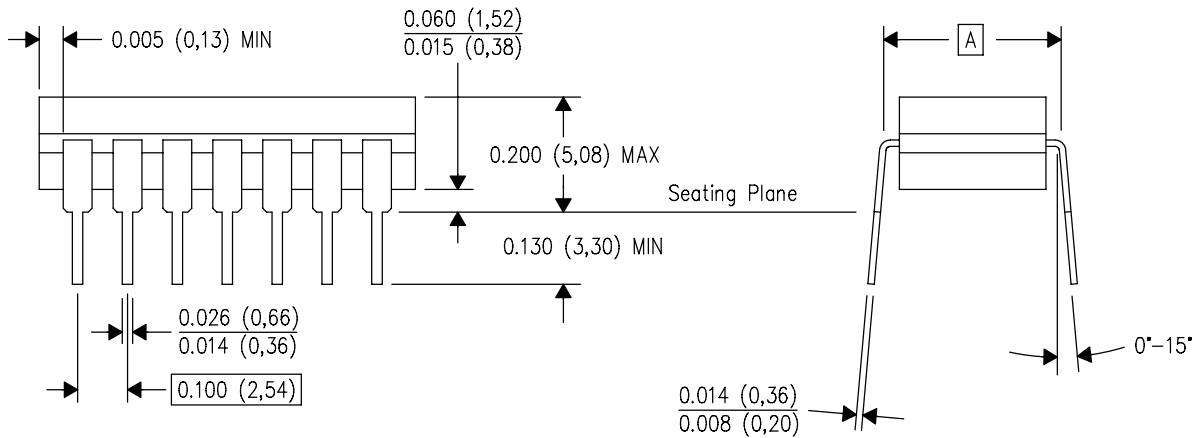
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14                     | 16                     | 18                     | 20                     |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A             | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX         | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN         | —                      | —                      | —                      | —                      |
| C MAX         | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN         | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



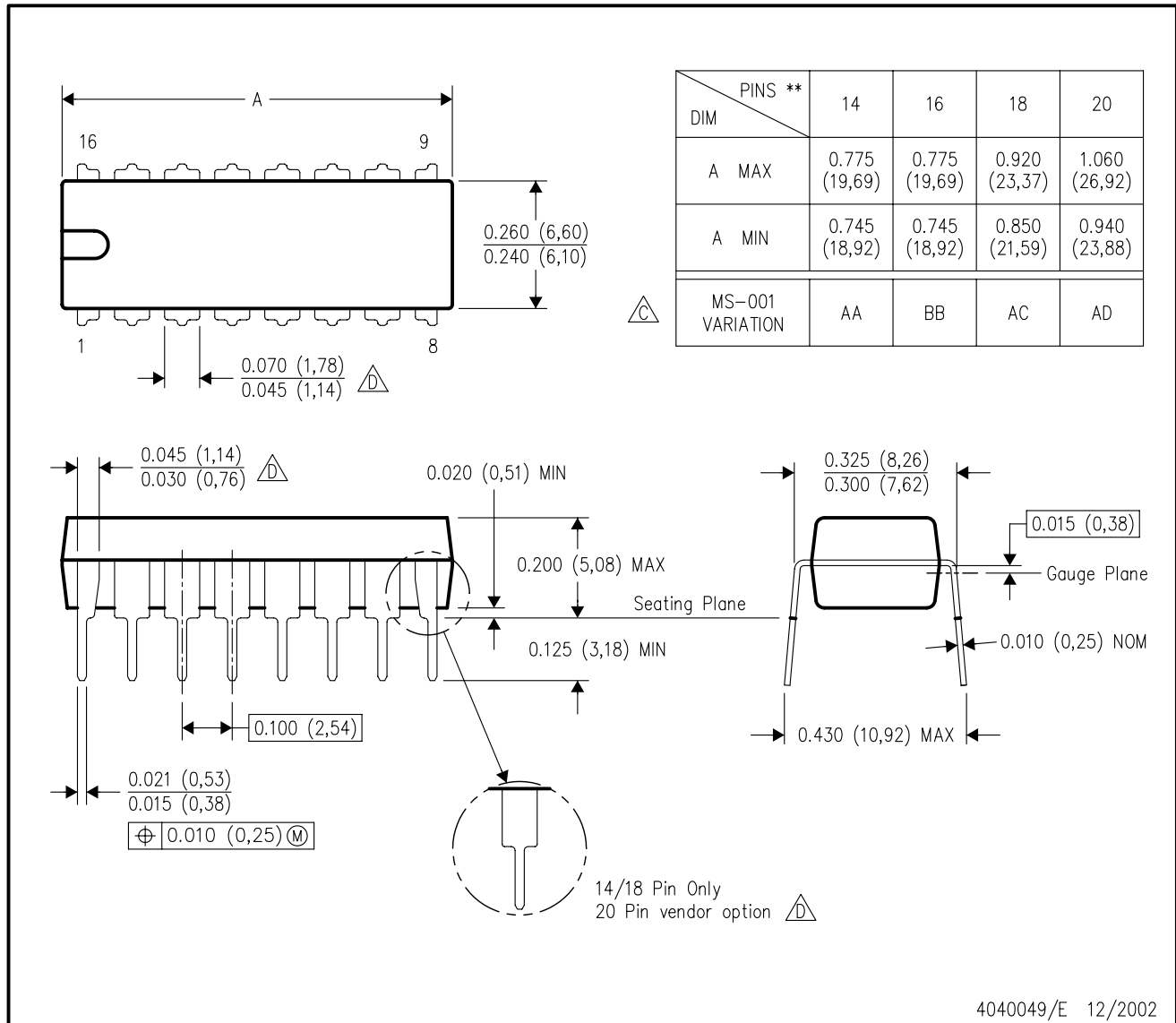
4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

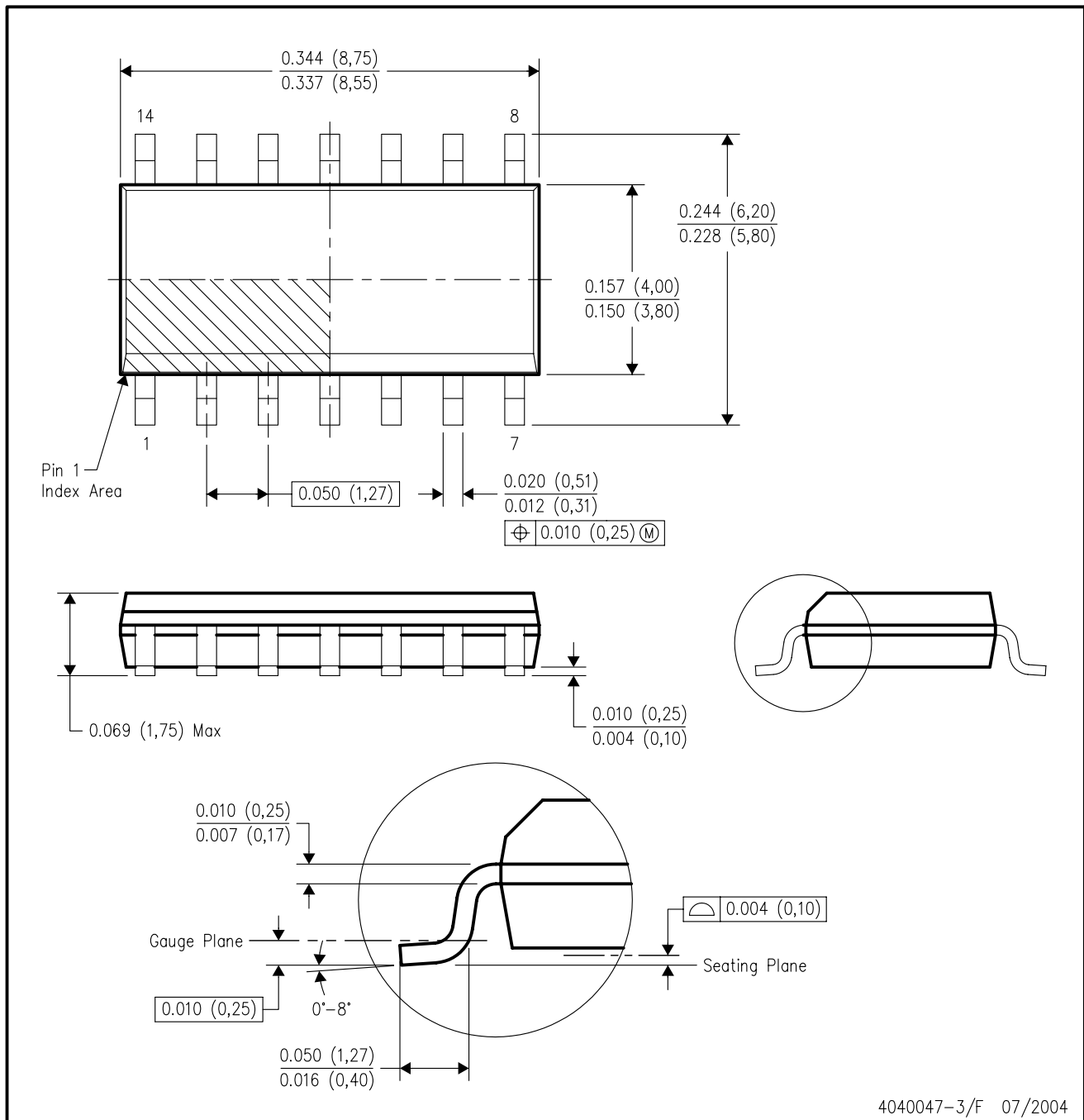
16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



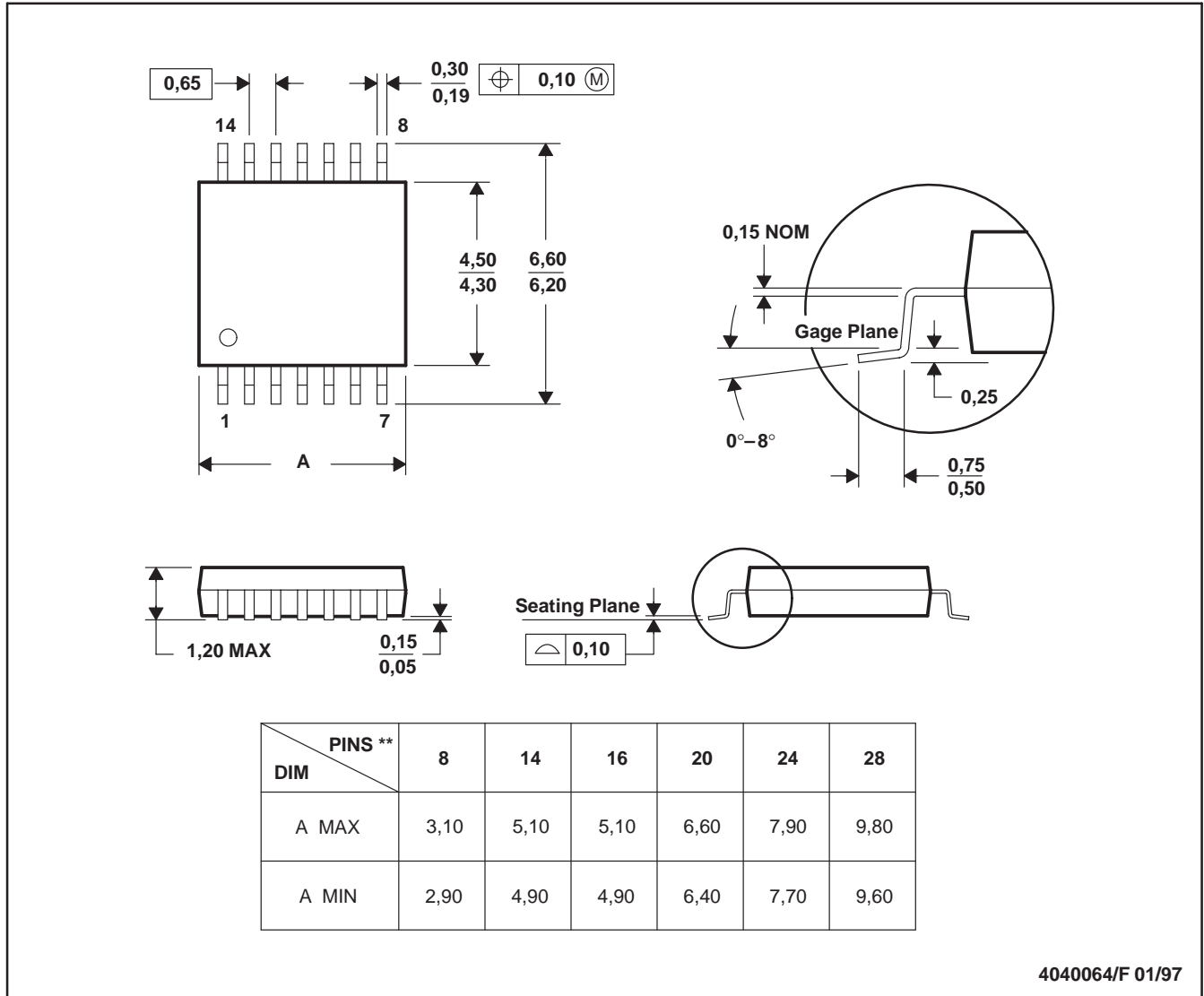
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-012 variation AB.



PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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