

SOJ, TSOP, FP-BGA  
Commercial Temp  
Industrial Temp

**128K x 8**  
**1Mb Asynchronous SRAM**

7, 8, 10, 12 ns  
3.3 V  $V_{DD}$   
Center  $V_{DD}$  and  $V_{SS}$

### Features

- Fast access time: 7, 8, 10, 12 ns
- CMOS low power operation: 140/120/95/80 mA at minimum cycle time
- Single 3.3 V power supply
- All inputs and outputs are TTL-compatible
- Fully static operation
- Industrial Temperature Option:  $-40^{\circ}$  to  $85^{\circ}\text{C}$
- Package line up
  - J: 400 mil, 32-pin SOJ package
  - TP: 400 mil, 32-pin TSOP Type II package
  - GP: Pb-Free 400 mil, 32-pin TSOP Type II package
  - SJ: 300 mil, 32-pin SOJ package
  - U: 6 mm x 8 mm Fine Pitch Ball Grid Array package
  - GU: Pb-Free 6 mm x 8 mm Fine Pitch Ball Grid Array package
- Pb-Free TSOP-II and FP-BGA packages available

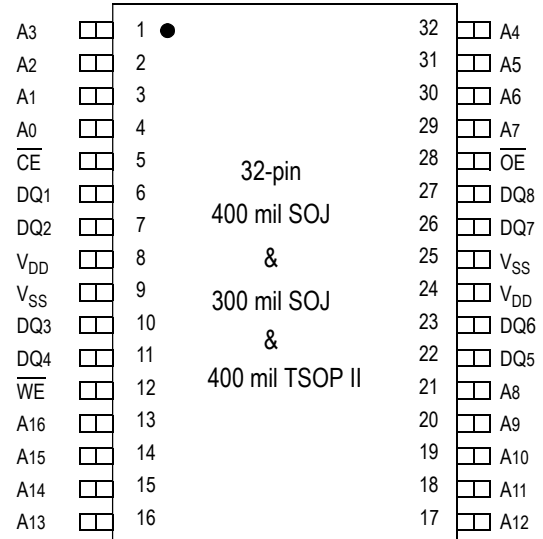
### Description

The GS71108A is a high speed CMOS Static RAM organized as 131,072 words by 8 bits. Static design eliminates the need for external clocks or timing strobes. The GS operates on a single 3.3 V power supply and all inputs and outputs are TTL-compatible. The GS71108A is available in a 6 mm x 8 mm Fine Pitch BGA package, as well as in 300 mil and 400 mil SOJ and 400 mil TSOP Type-II packages.

### Pin Descriptions

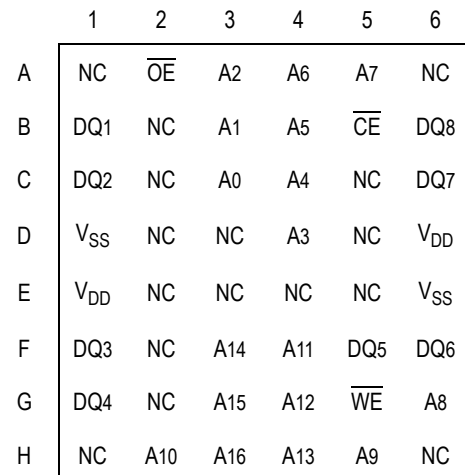
Symbol	Description
A <sub>0</sub> –A <sub>16</sub>	Address input
DQ <sub>1</sub> –DQ <sub>8</sub>	Data input/output
$\overline{\text{CE}}$	Chip enable input
$\overline{\text{WE}}$	Write enable input
$\overline{\text{OE}}$	Output enable input
$V_{DD}$	+3.3 V power supply
$V_{SS}$	Ground
NC	No connect

### SOJ & TSOP-II 128K x 8-Pin Configuration



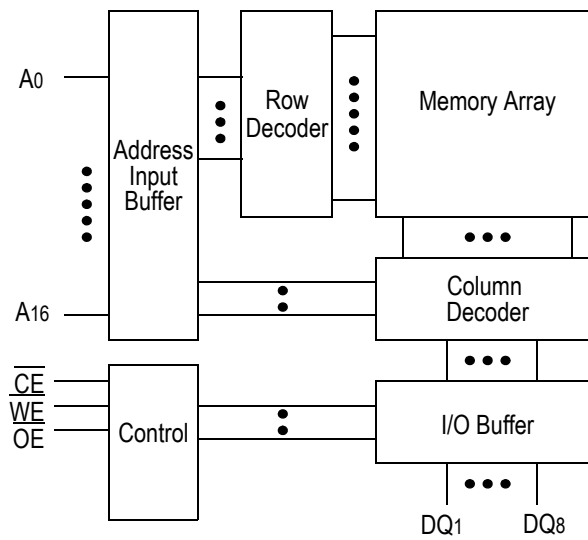
Packages J, TP, and SJ

### Fine Pitch BGA 128K x 8-Bump Configuration



Package U  
6 mm x 8 mm, 0.75 mm Bump Pitch  
Top View

Block Diagram



Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	DQ1 to DQ8	$V_{DD}$ Current
H	X	X	Not Selected	ISB1, ISB2
L	L	H	Read	IDD
L	X	L	Write	
L	H	H	High Z	

**Note:**  
X: "H" or "L"

### Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	$V_{DD}$	-0.5 to +4.6	V
Input Voltage	$V_{IN}$	-0.5 to $V_{DD} + 0.5$ ( $\leq 4.6$ V max.)	V
Output Voltage	$V_{OUT}$	-0.5 to $V_{DD} + 0.5$ ( $\leq 4.6$ V max.)	V
Allowable power dissipation	PD	0.7	W
Storage temperature	$T_{STG}$	-55 to 150	$^{\circ}C$

**Note:**

Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation shall be restricted to Recommended Operating Conditions. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

### Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage for -7/-8/-10/-12	$V_{DD}$	3.0	3.3	3.6	V
Input High Voltage	$V_{IH}$	2.0	—	$V_{DD} + 0.3$	V
Input Low Voltage	$V_{IL}$	-0.3	—	0.8	V
Ambient Temperature, Commercial Range	$T_{Ac}$	0	—	70	$^{\circ}C$
Ambient Temperature, Industrial Range	$T_{AI}$	-40	—	85	$^{\circ}C$

**Notes:**

1. Input overshoot voltage should be less than  $V_{DD} + 2$  V and not exceed 20 ns.
2. Input undershoot voltage should be greater than  $-2$  V and not exceed 20 ns.

## Capacitance

Parameter	Symbol	Test Condition	Max	Unit
Input Capacitance	$C_{IN}$	$V_{IN} = 0\text{ V}$	5	pF
Output Capacitance	$C_{OUT}$	$V_{OUT} = 0\text{ V}$	7	pF

### Notes:

1. Tested at  $T_A = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$
2. These parameters are sampled and are not 100% tested.

## DC I/O Pin Characteristics

Parameter	Symbol	Test Conditions	Min	Max
Input Leakage Current	$I_{IL}$	$V_{IN} = 0\text{ to }V_{DD}$	-1 $\mu\text{A}$	1 $\mu\text{A}$
Output Leakage Current	$I_{LO}$	Output High Z $V_{OUT} = 0\text{ to }V_{DD}$	-1 $\mu\text{A}$	1 $\mu\text{A}$
Output High Voltage	$V_{OH}$	$I_{OH} = -4\text{ mA}$	2.4	—
Output Low Voltage	$V_{OL}$	$I_{LO} = +4\text{ mA}$	—	0.4 V

## Power Supply Currents

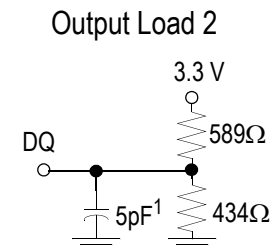
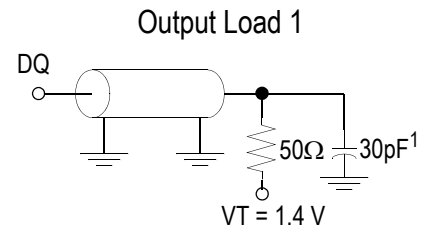
Parameter	Symbol	Test Conditions	0 to 70°C				-40 to 85°C			
			7 ns	8 ns	10 ns	12 ns	7 ns	8 ns	10 ns	12 ns
Operating Supply Current	$I_{DD}$	$\overline{CE} \leq V_{IL}$ All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Min. cycle time $I_{OUT} = 0\text{ mA}$	140 mA	120 mA	95 mA	80 mA	145 mA	125 mA	100 mA	85 mA
Standby Current	$I_{SB1}$	$\overline{CE} \geq V_{IH}$ All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Min. cycle time	25 mA	20 mA	20 mA	15 mA	30 mA	25 mA	25 mA	20 mA
Standby Current	$I_{SB2}$	$\overline{CE} \geq V_{DD} - 0.2\text{ V}$ All other inputs $\geq V_{DD} - 0.2\text{ V}$ or $\leq 0.2\text{ V}$	2 mA				5 mA			

**AC Test Conditions**

Parameter	Conditions
Input high level	$V_{IH} = 2.4\text{ V}$
Input low level	$V_{IL} = 0.4\text{ V}$
Input rise time	$t_r = 1\text{ V/ns}$
Input fall time	$t_f = 1\text{ V/ns}$
Input reference level	1.4 V
Output reference level	1.4 V
Output load	<b>Fig. 1 &amp; 2</b>

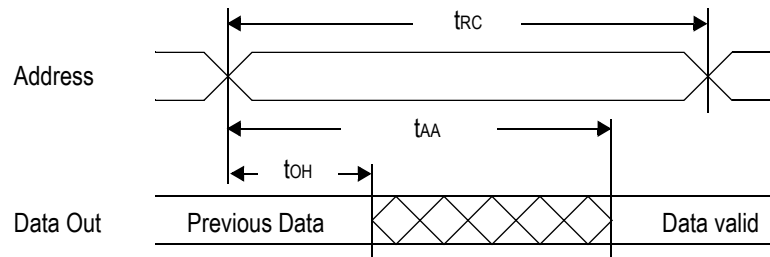
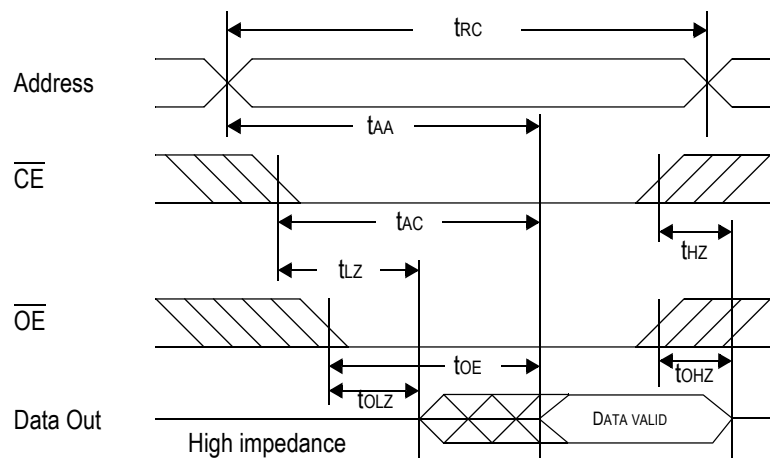
**Notes:**

1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in **Fig. 1** unless otherwise noted.
3. Output load 2 for  $t_{LZ}$ ,  $t_{HZ}$ ,  $t_{OLZ}$  and  $t_{OHZ}$


**AC Characteristics**
**Read Cycle**

Parameter	Symbol	-7		-8		-10		-12		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read cycle time	$t_{RC}$	7	—	8	—	10	—	12	—	ns
Address access time	$t_{AA}$	—	7	—	8	—	10	—	12	ns
Chip enable access time ( $\overline{CE}$ )	$t_{AC}$	—	7	—	8	—	10	—	12	ns
Output enable to output valid ( $\overline{OE}$ )	$t_{OE}$	—	3	—	3.5	—	4	—	5	ns
Output hold from address change	$t_{OH}$	3	—	3	—	3	—	3	—	ns
Chip enable to output in low Z ( $\overline{CE}$ )	$t_{LZ}^*$	3	—	3	—	3	—	3	—	ns
Output enable to output in low Z ( $\overline{OE}$ )	$t_{OLZ}^*$	0	—	0	—	0	—	0	—	ns
Chip disable to output in High Z ( $\overline{CE}$ )	$t_{HZ}^*$	—	3.5	—	4	—	5	—	6	ns
Output disable to output in High Z ( $\overline{OE}$ )	$t_{OHZ}^*$	—	3	—	3.5	—	4	—	5	ns

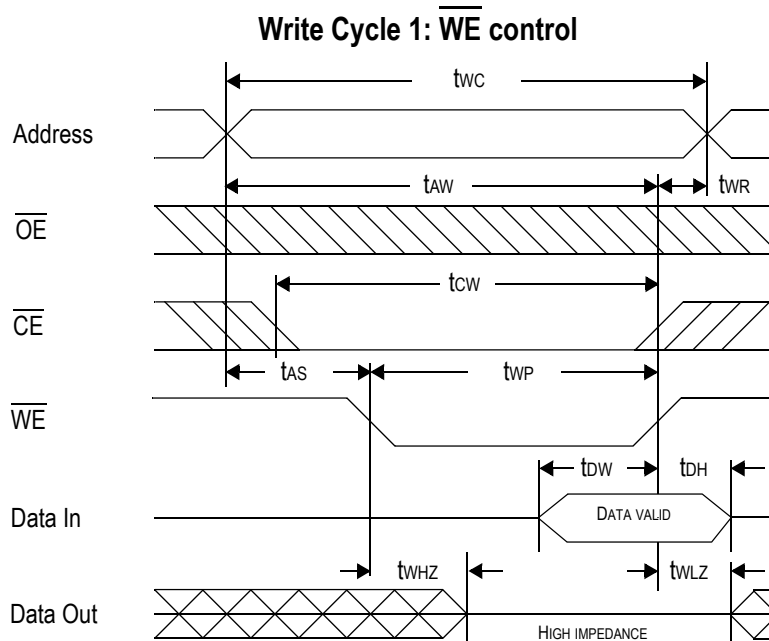
\* These parameters are sampled and are not 100% tested

**Read Cycle 1:  $\overline{CE} = \overline{OE} = V_{IL}$ ,  $\overline{WE} = V_{IH}$** 

**Read Cycle 2:  $\overline{WE} = V_{IH}$** 


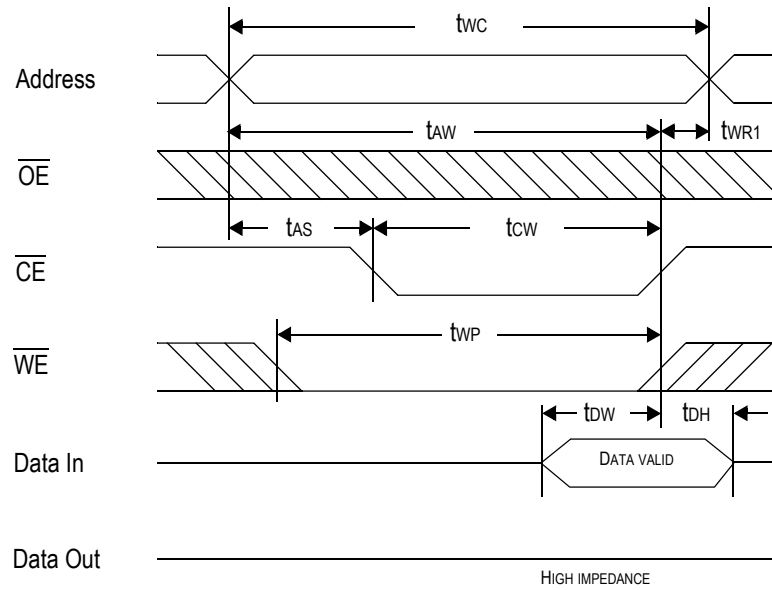
**Write Cycle**

Parameter	Symbol	-7		-8		-10		-12		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write cycle time	tWC	7	—	8	—	10	—	12	—	ns
Address valid to end of write	tAW	5	—	5.5	—	7	—	8	—	ns
Chip enable to end of write	tCW	5	—	5.5	—	7	—	8	—	ns
Data set up time	tDW	3	—	4	—	5	—	6	—	ns
Data hold time	tDH	0	—	0	—	0	—	0	—	ns
Write pulse width	tWP	5	—	5.5	—	7	—	8	—	ns
Address set up time	tAS	0	—	0	—	0	—	0	—	ns
Write recovery time ( $\overline{WE}$ )	tWR	0	—	0	—	0	—	0	—	ns
Write recovery time ( $\overline{CE}$ )	tWR1	0	—	0	—	0	—	0	—	ns
Output Low Z from end of write	tWLZ*	3	—	3	—	3	—	3	—	ns
Write to output in High Z	tWHZ*	—	3	—	3.5	—	4	—	5	ns

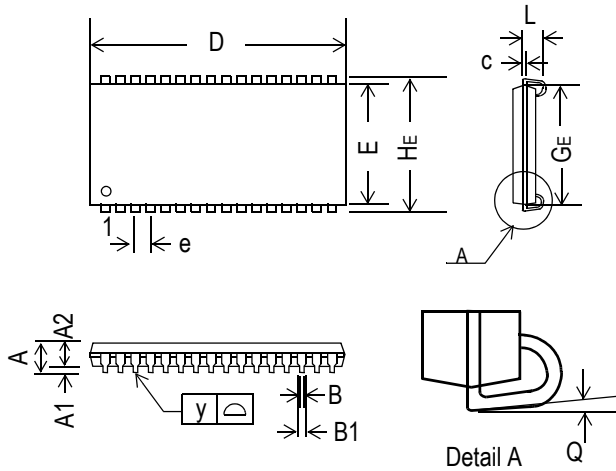
\* These parameters are sampled and are not 100% tested



Write Cycle 2:  $\overline{CE}$  control



32-Pin SOJ, 300 mil

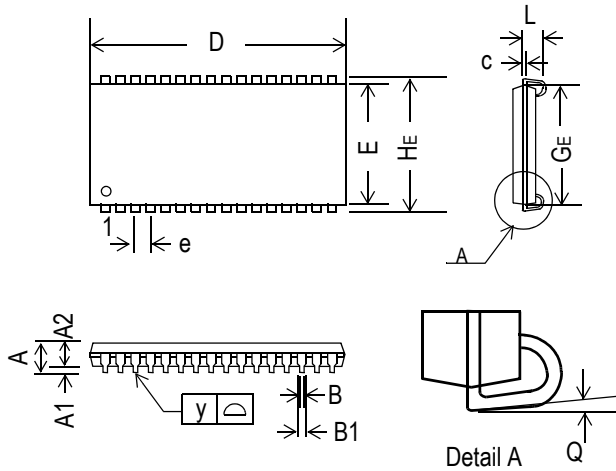


Symbol	Dimension in inch			Dimension in mm		
	min	nom	max	min	nom	max
A	0.125	—	0.148	3.175	—	3.76
A1	0.026	—	—	0.66	—	—
A2	0.095	0.100	0.105	2.41	2.54	2.67
B	0.013	0.017	0.021	0.33	0.43	0.53
B1	0.024	0.028	0.032	0.61	0.71	0.81
c	0.006	0.008	0.012	0.15	0.20	0.30
D	0.820	0.825	0.830	20.82	20.95	21.08
E	0.295	0.300	0.305	7.49	7.62	7.75
e	—	0.05	—	—	1.27	—
HE	0.330	0.335	0.340	8.38	8.51	8.64
GE	0.255	0.267	0.275	6.48	6.78	6.958
L	0.082	—	—	2.08	—	—
y	—	—	0.004	—	—	0.10
Q	0°	—	10°	0°	—	10°

**Notes:**

1. Dimension D & E do not include interlead flash.
2. Dimension B1 does not include dambar protrusion/intrusion.
3. Controlling dimension: inches

32-Pin SOJ, 400 mil

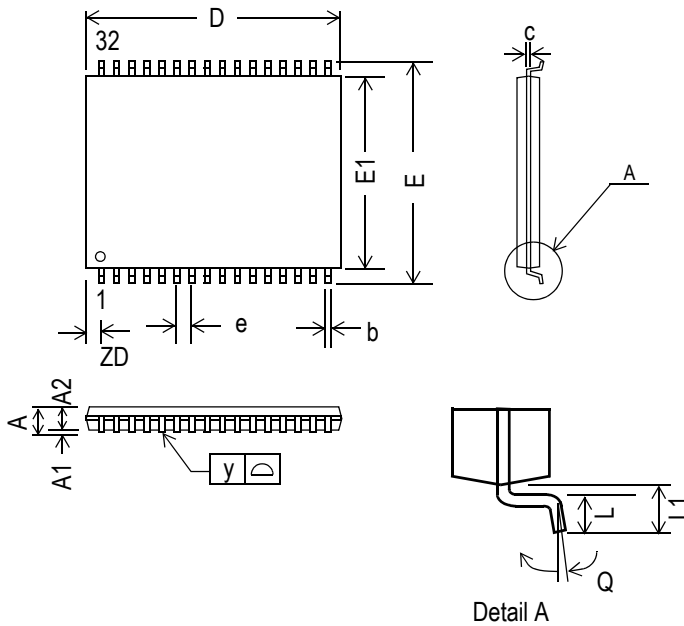


Symbol	Dimension in inch			Dimension in mm		
	min	nom	max	min	nom	max
A	—	—	0.146	—	—	3.70
A1	0.026	—	—	0.66	—	—
A2	0.105	0.110	0.115	2.67	2.80	2.92
B	0.013	0.017	0.021	0.33	0.43	0.53
B1	0.024	0.028	0.032	0.61	0.71	0.81
c	0.006	0.008	0.012	0.15	0.20	0.30
D	0.820	0.824	0.829	20.83	20.93	21.06
E	0.395	0.400	0.405	10.04	10.16	10.28
e	—	0.05	—	—	1.27	—
HE	0.430	0.435	0.440	10.93	11.05	11.17
GE	0.354	0.366	0.378	9.00	9.30	9.60
L	0.082	—	—	2.08	—	—
y	—	—	0.004	—	—	0.10
Q	0°	—	10°	0°	—	10°

**Notes:**

1. Dimension D & E do not include interlead flash.
2. Dimension B1 does not include dambar protrusion/intrusion.
3. Controlling dimension: inches

32-Pin TSOP-II, 400mil

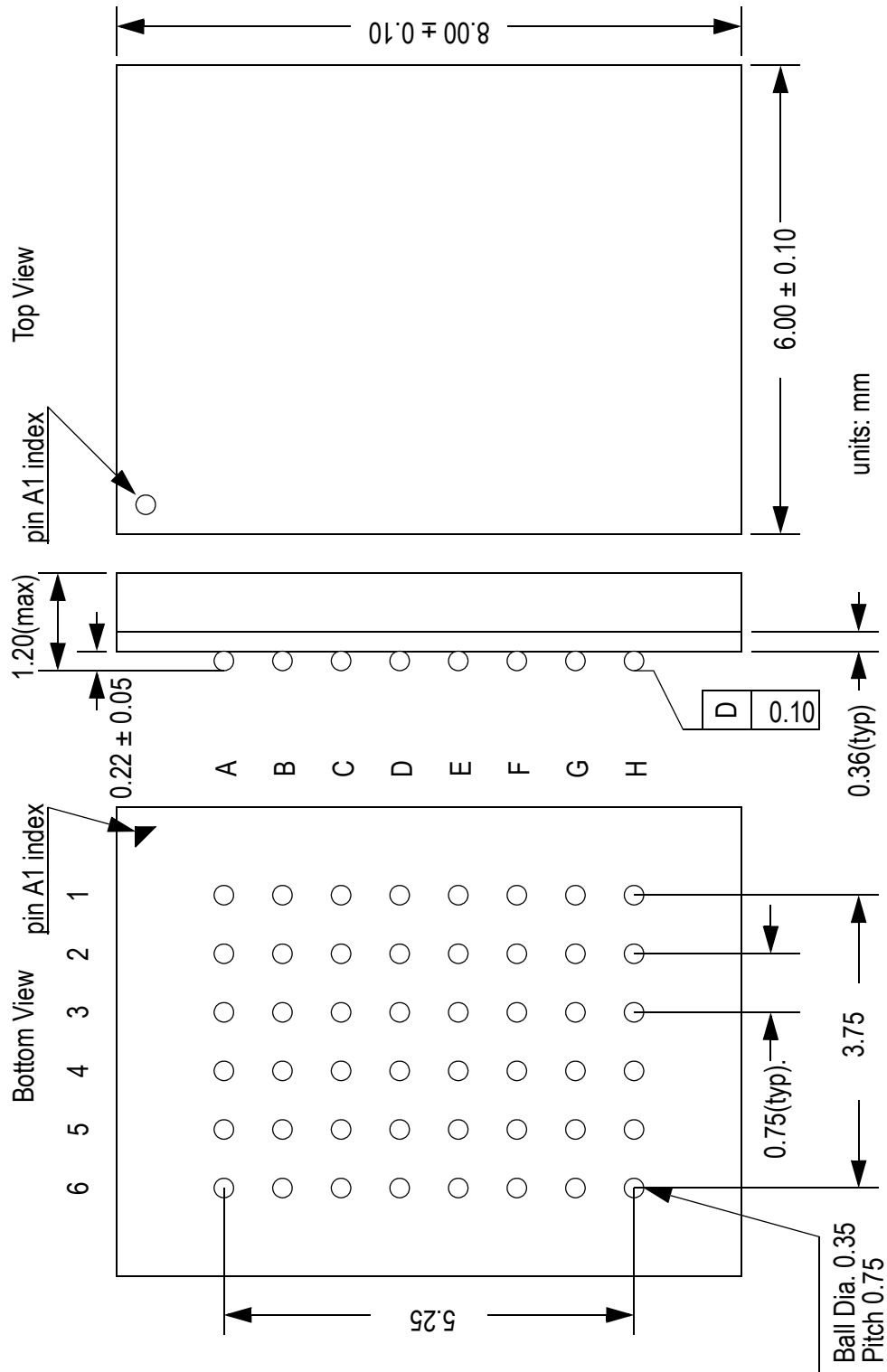


Symbol	Dimension in inch			Dimension in mm		
	min	nom	max	min	nom	max
A	0.039	—	0.05	—	—	1.27
A1	0.002	—	0.006	0.01	—	0.15
A2	0.037	0.040	0.045	0.90	1.02	1.14
b	0.012	0.016	0.018	0.30	0.40	0.45
c	0.0047	0.0051	0.0062	0.12	0.13	0.16
D	0.820	0.825	0.830	20.82	20.95	21.08
ZD	—	0.037	—	—	0.95	—
E	0.455	0.463	0.471	11.56	11.76	11.96
E1	0.395	0.400	0.405	10.03	10.16	10.29
e	—	0.05	—	—	1.27	—
L	0.017	0.020	0.023	0.40	0.50	0.60
L1	0.024	0.031	0.039	0.60	0.80	1.00
y	0.00	—	0.003	0.00	—	0.76
Q	0°	—	5°	0°	—	5°

**Notes:**

1. Dimension D includes mold flash, protrusions or gate burrs.
2. Dimension E does not include interlead flash
3. Controlling dimension: mm

6 mm x 8 mm Fine Pitch BGA



**Ordering Information**

<b>Part Number*</b>	<b>Package</b>	<b>Access Time</b>	<b>Temp. Range</b>	<b>Status</b>
GS71108ATP-7	400 mil TSOP-II	7 ns	Commercial	
GS71108ATP-8	400 mil TSOP-II	8 ns	Commercial	
GS71108ATP-10	400 mil TSOP-II	10 ns	Commercial	
GS71108ATP-12	400 mil TSOP-II	12 ns	Commercial	
GS71108ATP-7I	400 mil TSOP-II	7 ns	Industrial	
GS71108ATP-8I	400 mil TSOP-II	8 ns	Industrial	
GS71108ATP-10I	400 mil TSOP-II	10 ns	Industrial	
GS71108ATP-12I	400 mil TSOP-II	12 ns	Industrial	
GS71108AGP-7	Pb-free 400 mil TSOP-II	7 ns	Commercial	
GS71108AGP-8	Pb-free 400 mil TSOP-II	8 ns	Commercial	
GS71108AGP-10	Pb-free 400 mil TSOP-II	10 ns	Commercial	
GS71108AGP-12	Pb-free 400 mil TSOP-II	12 ns	Commercial	
GS71108AGP-7I	Pb-free 400 mil TSOP-II	7 ns	Industrial	
GS71108AGP-8I	Pb-free 400 mil TSOP-II	8 ns	Industrial	
GS71108AGP-10I	Pb-free 400 mil TSOP-II	10 ns	Industrial	
GS71108AGP-12I	Pb-free 400 mil TSOP-II	12 ns	Industrial	
GS71108ASJ-7	300 mil SOJ	7 ns	Commercial	
GS71108ASJ-8	300 mil SOJ	8 ns	Commercial	
GS71108ASJ-10	300 mil SOJ	10 ns	Commercial	
GS71108ASJ-12	300 mil SOJ	12 ns	Commercial	
GS71108ASJ-7I	300 mil SOJ	7 ns	Industrial	
GS71108ASJ-8I	300 mil SOJ	8 ns	Industrial	
GS71108ASJ-10I	300 mil SOJ	10 ns	Industrial	
GS71108ASJ-12I	300 mil SOJ	12 ns	Industrial	
GS71108AJ-7	400 mil SOJ	7 ns	Commercial	
GS71108AJ-8	400 mil SOJ	8 ns	Commercial	
GS71108AJ-10	400 mil SOJ	10 ns	Commercial	
GS71108AJ-12	400 mil SOJ	12 ns	Commercial	
GS71108AJ-7I	400 mil SOJ	7 ns	Industrial	
GS71108AJ-8I	400 mil SOJ	8 ns	Industrial	

**Ordering Information**

<b>Part Number *</b>	<b>Package</b>	<b>Access Time</b>	<b>Temp. Range</b>	<b>Status</b>
GS71108AJ-10I	400 mil SOJ	10 ns	Industrial	
GS71108AJ-12I	400 mil SOJ	12 ns	Industrial	
GS71108AU-7	6 mm x 8 mm Fine Pitch BGA	7 ns	Commercial	
GS71108AU-8	6 mm x 8 mm Fine Pitch BGA	8 ns	Commercial	
GS71108AU-10	6 mm x 8 mm Fine Pitch BGA	10 ns	Commercial	
GS71108AU-12	6 mm x 8 mm Fine Pitch BGA	12 ns	Commercial	
GS71108AU-7I	6 mm x 8 mm Fine Pitch BGA	7 ns	Industrial	
GS71108AU-8I	6 mm x 8 mm Fine Pitch BGA	8 ns	Industrial	
GS71108AU-10I	6 mm x 8 mm Fine Pitch BGA	10 ns	Industrial	
GS71108AU-12I	6 mm x 8 mm Fine Pitch BGA	12 ns	Industrial	
GS71108AGU-7	Pb-free 6 mm x 8 mm Fine Pitch BGA	7 ns	Commercial	
GS71108AGU-8	Pb-free 6 mm x 8 mm Fine Pitch BGA	8 ns	Commercial	
GS71108AGU-10	Pb-free 6 mm x 8 mm Fine Pitch BGA	10 ns	Commercial	
GS71108AGU-12	Pb-free 6 mm x 8 mm Fine Pitch BGA	12 ns	Commercial	
GS71108AGU-7I	Pb-free 6 mm x 8 mm Fine Pitch BGA	7 ns	Industrial	
GS71108AGU-8I	Pb-free 6 mm x 8 mm Fine Pitch BGA	8 ns	Industrial	
GS71108AGU-10I	Pb-free 6 mm x 8 mm Fine Pitch BGA	10 ns	Industrial	
GS71108AGU-12I	Pb-free 6 mm x 8 mm Fine Pitch BGA	12 ns	Industrial	

\* Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. For example: GS71108ATP-8T

**1Mb Asynchronous Datasheet Revision History**

Rev. Code: Old; New	Types of Changes Format or Content	Page #/Revisions/Reason
71108A_r1		• Creation of new datasheet
71108A_r1; 71108A_r1_01	Content	• Added 6 ns speed bin to entire document
71108A_r1_01; 71108A_r1_02	Content	• Updated all power numbers • Changed 6 mm x 10 mm package designator from U to X
71108A_r1_02; 71108A_r1_03	Content	• Updated Recommended Operating Conditions table on page 3 • Updated Power Supply Currents table • Changed FPBGA package from 6 x 10 to 6 x 8 (package U)
71108A_r1_03; 71108A_r1_04	Content	• Removed 6 ns speed bin from entire document • Added 7 ns speed bin to entire document
71108A_r1_04; 71108A_r1_05	Content	• Added missing 300 mil SOJ mechanical drawing
71108A_r1_05; 71108A_r1_06	Content	• Updated format • Added Pb-free information for TSOP-II package
71108A_r1_06; 71108A_r1_07	Content	• Added Pb-free information for FP-BGA package